HITACHI DOT MATRIX LIQUID CRYSTAL DISPLAY MODULE

HITACHI

PREFACE

Hitachi Dot Matrix Liquid Crystal Display Module (LCM) uses bright and high-contrast twist-nematic liquid crystal and is available for display of numerals, alphabets, Chinese & Japanese characters, symbols and graphics.

Due to its small size, light weight, low voltage, low power consumption, easy handling, etc., the Hitachi Dot Matrix LCD Module has been used widely as display component for portable data terminal equipment, word processors and high class electronic tabletop calculators in Japan and abroad.

This catalog describes the electrical and optical characteristics, external dimensions and precautions in handling the standard type of the product which should be helpful when selecting and designing equipment.

- **Notes**

When using this catalog, the reader should keep the following in mind:

1. This catalog may, wholly or partially, be subject to change without notice.
2. This catalog neither ensures the enforcement of any industrial properties on other rights, nor sanctions the enforcement right thereof.
   Examples of circuit given in this catalog are only for better understanding of the products. Therefore, Hitachi will not be responsible for any accidents or problems caused during operation of his unit according to this catalog.
3.

CONTENTS

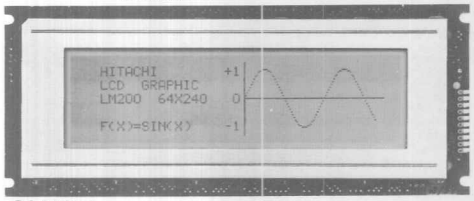
PHOTOGRAPHS OF LCD MODULE PRODUCTS

• GRAPHIC LCD MODULE

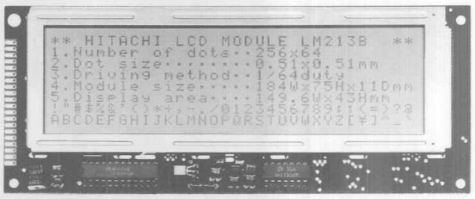
●H2525

●LM021

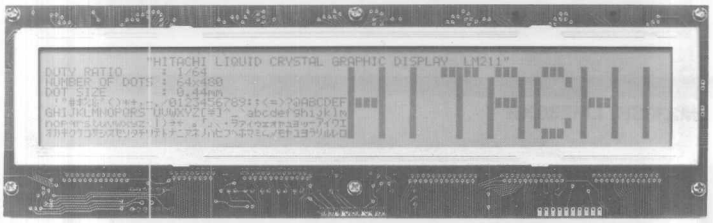
●LM212



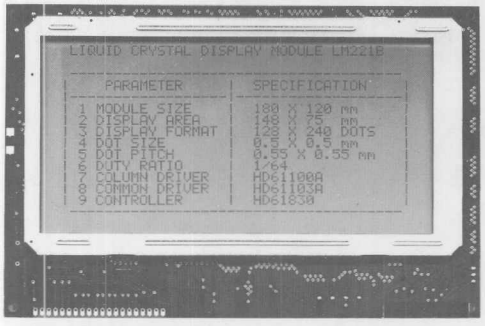
●LM200



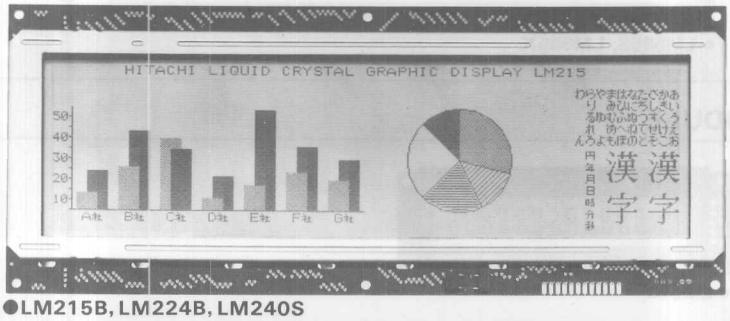
●LM213B



●LM211

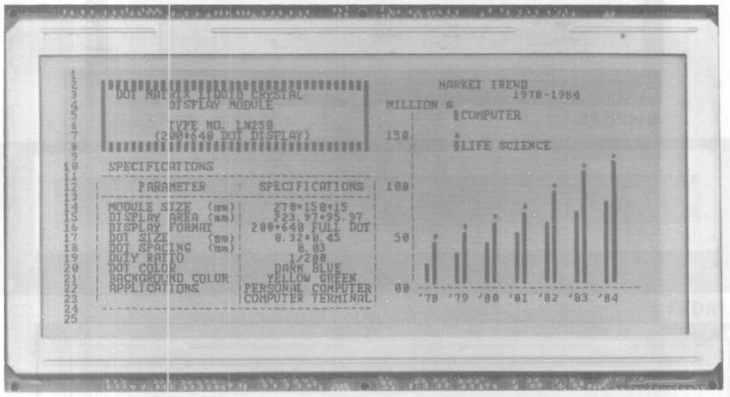


●LM221B, LM238B

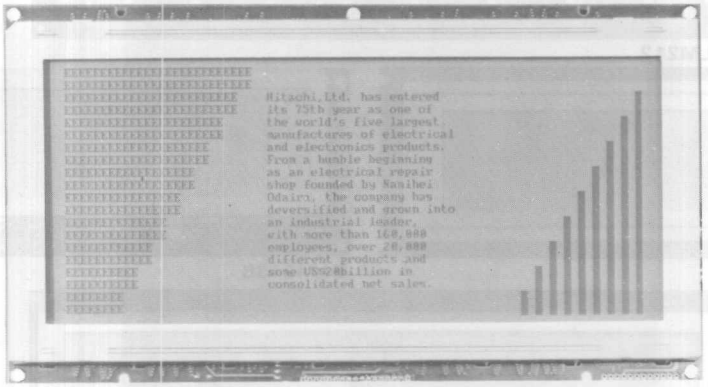


●LM215B, LM224B, LM240S

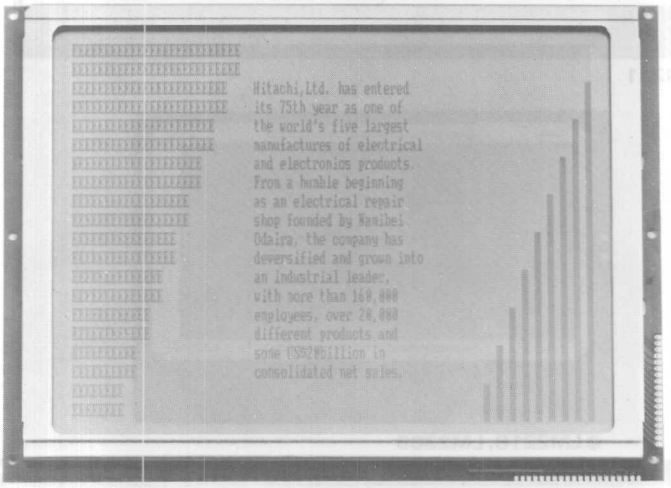
APPEARANCE



• LM225S, LM225X

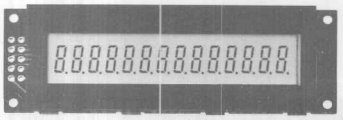


• LM236SB, LM236XB



• LM585S, LM585X

SEGMENT TYPE LCD MODULE

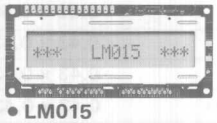


• LM039

• LCD MODULE WITH BUILT-IN CONTROLLER LSI

• LM054

• H2570



• LM015

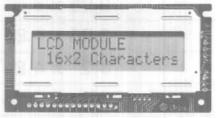
• LM568AF

• LM027

• LM020L

• LM070L

• LM052L



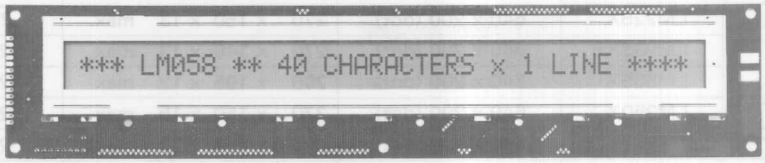
• LM016L

• LM038

• H2571

• H2572

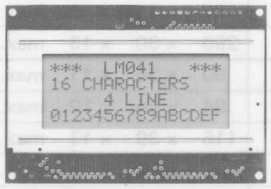
• LM032



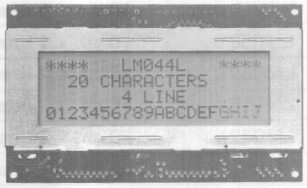
• LM058

• LM017L

• LM018L



• LM041L

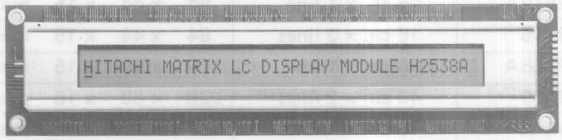


• LM044L

• LCD MODULE WITH ATTACHABLE CONTROLLER LSI

• H2532A

• H2535



• H2538A

• H2539

TABULATED DATA FOR HITACHI DOT MATRIX LIQUID CRYSTAL

Type			Type No.	No. of display W x H	External dimensions W x H x T (mm)	Effective viewing area W x H (mm)	Character dimensions W x H (mm)	Driving method (Duty)
Graphic display module			H2525	239 x 20 (dot)	220 x 53 x 15 max.	163 x 17	0.55 x 0.55*	1/20
			LM021	479 x 24 (dot)	290 x 60 x 13 max.	245 x 19	0.43 x 0.55*	1/24
			LM212	640 x 48 (dot)	270 x 63 x 13.8 max.	241 x 25	0.32 x 0.38*	1/48
			LM200	240 x 64 (dot)	180 x 75 x 13.8 max.	132 x 39	0.48 x 0.48*	1/32
			LM213B	256 x 64 (dot)	184 x 75 x 12 max.	149.6 x 43	0.51 x 0.51*	1/64
			LM211B	480 x 64 (dot)	270 x 82 x 13 max.	240 x 38	0.44 x 0.44*	1/64
			LM221B	240 x 128 (dot)	180 x 120 x 13.8 max.	148 x 75	0.50 x 0.50*	1/64
			LM238B	240 x 128 (dot)	180 x 120 x 13.8 max.	148 x 75	0.50 x 0.50*	1/64
			LM215B	480 x 128 (dot)	270 x 110 x 11.5 max.	242 x 69	0.43 x 0.43*	1/64
			LM215SB	480 x 128 (dot)	270 x 110 x 11.5 max.	242 x 69	0.43 x 0.43*	1/64
			LM224B	480 x 128 (dot)	Same as LM215B, only the display is divided into 2 blocks.		0.43 x 0.43*	1/64
			LM225S	640 x 200 (dot)	270 x 150 x 13 max.	239 x 104	0.32 x 0.46*	1/100
			LM240S	480 x 128 (dot)	270 x 110 x 11.5 max.	242 x 69	0.43 x 0.43*	1/128
			LM236SB	640 x 200 (dot)	270 x 149 x 13 max.	239 x 104	0.32 x 0.46*	1/100
			LM585S	640 x 200 (dot)	260 x 195 x 12.5 max.	220 x 166	0.29 x 0.74*	1/100
		Under-development	LM225X	640 x 200 (dot)	270 x 150 x 13 max.	239 x 104	0.32 x 0.46*	1/100
			LM236XB	640 x 200 (dot)	270 x 149 x 13 max.	239 x 104	0.32 x 0.46*	1/100
			LM585X	640 x 200 (dot)	260 x 195 x 12 max.	220 x 166	0.29 x 0.74*	1/100
			LM250X	640 x 200 (dot)	270 x 150 x 15 max.	239 x 104	0.32 x 0.46*	1/200
			LM252X	640 x 400 (dot)	270 x 198 x 13.5 max.	236 x 153.6	0.33 x 0.33*	1/200
Character display module	With built-in controller LSI	1 line series	LM054	8 ch. x 1 line	84 x 44 x 12 max.	61 x 15.8	6.45 x 9.4	1/8
			H2570	16 ch. x 1 line	80 x 36 x 12 max.	64.5 x 13.8	3.15 x 7.9	1/11
			LM015	16 ch. x 1 line	80 x 36 x 12 max.	64.5 x 13.8	3.15 x 5.5	1/8
			LM568AF	16 ch. x 1 line	122 x 33 x 12 max.	99.0 x 13.0	4.84 x 8.06	1/8
			LM020L	16 ch. x 1 line	80 x 36 x 12 max.	64.5 x 13.8	3.07 x 5.73	1/16
			LM070L	20 ch. x 1 line	105 x 39.0 x 11 max.	84.0 x 13.0	3.2 x 5.2	1/8
			LM038	20 ch. x 1 line	182 x 35.5 x 13 max.	154.0 x 15.3	6.7 x 9.4	1/8
			LM027	24 ch. x 1 line	126 x 36 x 12 max.	100 x 13.8	3.15 x 7.9	1/11
			H2571	32 ch. x 1 line	174.5 x 33 x 13.4 max.	132.5 x 14	3.15 x 7.9	1/11
			H2572	40 ch. x 1 line	182 x 35.5 x 13 max.	154.0 x 15.3	3.15 x 7.9	1/11
			LM058	40 ch. x 1 line	290 x 60 x 13 max.	245.0 x 19.0	4.82 x 8.18	1/8
		2 lines series	LM052L	16 ch. x 2 lines	80 x 36 x 11 max.	64.5 x 13.8	2.95 x 3.8	1/16
			LM016L	16 ch. x 2 lines	84 x 44 x 12 max.	61 x 15.8	2.96 x 4.86	1/16
			LM032L	20 ch. x 2 lines	116 x 39 x 13 max.	83 x 18.6	3.2 x 4.85	1/16
			LM060L	24 ch. x 2 lines	116 x 39 x 13 max.	83 x 18.6	2.7 x 4.85	1/16
			LM017L	32 ch. x 2 lines	174.5 x 33 x 13.4 max.	141.2 x 16.75	3.45 x 4.85	1/16
			LM018L	40 ch. x 2 lines	182 x 35.5 x 13 max.	154.0 x 15.3	3.2 x 4.85	1/16
		4 line series	LM041L	16 ch. x 4 lines	87 x 60 x 12 max.	61.8 x 25.2	2.95 x 4.15	1/16
			LM044L	20 ch. x 4 lines	98 x 60 x 12 max.	76 x 25.2	2.95 x 4.15	1/16
	Controller LSI attachable		H2532A	16 ch. x 1 line	84 x 44 x 15 max.	61 x 15.8	2.9 x 5.5	1/8
			H2535	16 ch. x 2 lines	84 x 44 x 15 max.	61 x 15.8	2.9 x 4.1	1/16
			H2538A	40 ch. x 1 line	220 x 50 x 15 max.	163 x 17	3.15 x 5.5	1/8
			H2539	40 ch. x 2 lines	220 x 50 x 15 max.	163 x 17	3.15 x 4.45	1/16
Segment type			LM039	16 ch. x 1 line	87 x 27.5 x 11 max.	64.7 x 13.3	2.2 x 6.4	1/4
Option			Transflective type (T type) and character display type LCM with an extended temperature range (operation: −10°C ~ 70°C; storage: −40°C ~ 80°C) (H type) are also available on request. (LM016LT, H2570H etc.) See page 12 for details.					

* : Dot size ■ Underdevelopment

DISPLAY MODULE

Recommended power supply		Power consumption Typ. (mW)	Operating temperature (°C)	Storage temperature (°C)	Weight (g)	Power supply	Built-in LSI	Recommended controller LSI
$V_{DD}-V_{SS}$ (V)	$V_{EE}-V_{SS}$ (V)							
+5	−5	20	0 ~ +50	−20 ~ +60	100	Double	HD44104	HD61830
+5	−5	30	0 ~ +50	−20 ~ +60	150		HD44100	(CB1020R)
+5	–	50	0 ~ +40	−20 ~ +60	170	Single	MSM5839	HD61830 (CB1030R)
+5	−5	25	0 ~ +50	−20 ~ +60	150	Double	HD44104	HD61830 (CB1020R)
+5	−9	250	0 ~ +40	−20 ~ +60	180		HD61830 + HD44104	Built-in
+5	−9	130	0 ~ +40	−20 ~ +60	180		MSM5839/5238	HD61830
+5	−13.5	130	0 ~ +50	−20 ~ +60	210		HD61100/03	(CB1026R)
+5	−13.5	250	0 ~ +50	−20 ~ +60	220		HD61100/03	Built-in
+5	−10	100	0 ~ +50	−20 ~ +60	320		HD61100/03	HD61830 (CB1030R)
+5	−10	100	0 ~ +50	−20 ~ +60	320			
+5	−11	100	0 ~ +50	−20 ~ +60	320		HD61100/03	HD61830B
+5	−13.5	400	0 ~ +50	−20 ~ +60	450		HD61100/03	HD61830B (CB1040R)
+5	−14.5	120	0 ~ +50	−20 ~ +60	320		MSM5279/78	MSM6255
+5	−14.5	170	0 ~ +50	−20 ~ +60	450			
+5	−14.5	170	0 ~ +50	−20 ~ +60	540			
+5	−13.5	70	0 ~ +40	−20 ~ +60	450	Double	HD61100/03	HD61830B
+5	−15	105	0 ~ +40	−20 ~ +60	450		MSM5279/78	MSM6255G
+5	−14.5	105	0 ~ +40	−20 ~ +60	540			
+5	−20	190	0 ~ +40	−20 ~ +60	450		HD61104/05	HD63645F■
+5	−20	190	0 ~ +40	−20 ~ +60	580			
+5	–	10	0 ~ +50	−20 ~ +70	25	Single	HD44780	Built-in
+5	–	10	0 ~ +50	−20 ~ +70	25		HD44780 + HD44100 or MSM5259	
+5	–	10	0 ~ +50	−20 ~ +70	25			
+5	–	10	0 ~ +50	−20 ~ +70	25			
+5	–	10	0 ~ +50	−20 ~ +70	25		HD44780	
+5	–	10	0 ~ +50	−20 ~ +70	40			
+5	–	10	0 ~ +50	−20 ~ +70	65		HD44780 + HD44100 or MSM5259	
+5	–	10	0 ~ +50	−20 ~ +70	40			
+5	–	10	0 ~ +50	−20 ~ +70	60			
+5	–	10	0 ~ +50	−20 ~ +70	65			
+5	–	10	0 ~ +50	−20 ~ +70	150			
+5	–	15	0 ~ +50	−20 ~ +70	25	Single	HD44780 + HD44100 or MSM5259	Built-in
+5	–	15	0 ~ +50	−20 ~ +70	25			
+5	–	15	0 ~ +50	−20 ~ +70	50			
+5	–	15	0 ~ +50	−20 ~ +70	60			
+5	–	15	0 ~ +50	−20 ~ +70	60			
+5	–	15	0 ~ +50	−20 ~ +70	65			
+5	–	15	0 ~ +50	−20 ~ +70	60	Single	HD44780 + HD44104	Built-in
+5	–	17.5	0 ~ +50	−20 ~ +70	65			
+5	−5	15	0 ~ +50	−20 ~ +60	25	Double	HD44100	HD43160AH
+5	−5	10	0 ~ +50	−20 ~ +60	25			
+5	−5	10	0 ~ +50	−20 ~ +60	100			
+5	−5	10	0 ~ +50	−20 ~ +60	100			
+5	–	1.05	0 ~ +50	−20 ~ +70	20	Single	μPD7225G	Built-in

FEATURES

1. Various types are available, from small-size module for character display, to large-size module for graphic display.
2. An LSI is loaded exclusively for the LCD element drive. Also, a type containing a controller LSI is available.
3. When using graphic liquid crystal display module, use our recommendable control circuit board that simplifies the display system.
4. Due to its small size and light weight, compact display equipment can be constructed.
5. Due to low driving voltage and low power consumption, it can be driven by battery.

APPLICATIONS

1. Portable data terminal equipment
2. Word processors
3. Telephone applications
4. Facsimile machines
5. Handy personal computers
6. POS terminal equipment
7. Electronic typewriters
8. Measuring instruments
9. Other display devices

MAXIMUM RATINGS

Electric maximum ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply for logic	$V_{DD} - V_{SS}$	Refer to individual specification		V	
Power supply for LCD drive	$V_{DD} - V_O$			V	
Input voltage	V_I			V	
Static electricity		–	100	V	Note (1)

Note (1) Test and conditions of resistance to static electricity. After the condenser with a capacity of 200 pF is charged with recommended voltage, it is discharged by contact with interface connector pin.

Environmental conditions

Item	Operating		Non-operating		Remarks
	Min.	Max.	Min.	Max.	
Ambient temperature	Refer to individual specifications				No dew
Humidity	Note (2)				
Vibration	–	0.5G	–	2G	
Shock	–	3G	–	50G	XYZ 3 directions
Corrosion gas	No corrosion gas				

Note (2) Humidity conditions are as follows.

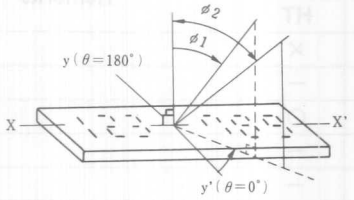
Number of dots / Ambient temperature (Ta)	Below 128 x 240	128 x 240 or over
Ta ≦ 40°C	95% RH max.	85% RH max.
Ta > 40°C (Below maximum temperature)	Below maximum absolute humidity of 40°C 95% RH	Below maximum absolute humidity of 40°C 85% RH

OPTICAL DATA

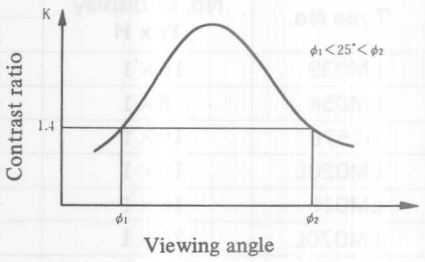
Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing angle	$\phi 2-\phi 1$	K=1.4	20	–	–	deg.	1, 2, 8
Contrast ratio	K	$\phi=25°$ $\theta=0°$	–	3	–	–	3
Response time (rise)	t_r	$\phi=25°$ $\theta=0°$	–	200	400	ms	4, 5
				250	400		4, 6
				150	250		4, 7
Response time (fall)	t_f	$\phi=25°$ $\theta=0°$	–	200	400	ms	4, 5
				250	400		4, 6
				150	250		4, 7

Note 1. Definition of θ and ϕ

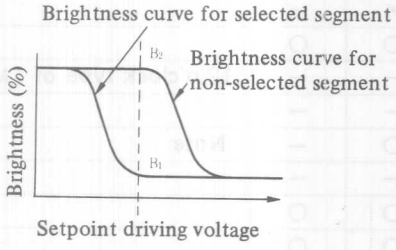


Note 2. Definition of viewing angle $\phi 1$, and $\phi 2$

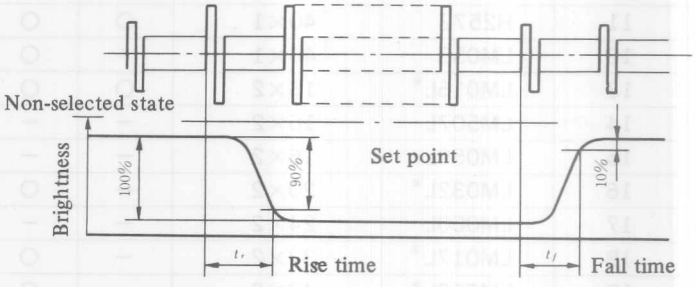


Note 3. Definition of contrast "K"

$$K = \frac{\text{Brightness of non-selected segment } (B_2)}{\text{Brightness of selected segment } (B_1)}$$



Note 4. Definition of optical response



Note 5. Applied types
H2532A · H2535 · H2538A · H2568

Note 6. Applied types
LM054 · LM020L · LM038 · H2539 · H2570 · LM015 · LM027 · H2571 · H2572 · LM016L · LM032L · LM017L · LM018L · LM041L · LM044L · LM052L · LM568AF · LM070L · LM060L

Note 7. Applied types
H2525 · LM200 · LM021 · LM213B · LM211B · LM212 · LM215 · LM039

Note 8. Typical viewing angle of following types is 20 deg.
LM200 · LM213B · LM211B · LM212 · LM215B · LM224B · LM225S · LM236SB

SEMICUSTOM

We provide liquid crystal module with optional specifications as follows. Table 1 shows LCD module already in production.

(1) Types of optional specifications (A, T, H, L comes at the end of each type. Provided, when "H" option is required for types with *, "L" at the end comes off and "H" is added instead, for example, LM016L becomes LM016H).

A: Black coated front panel (metal frame)
T: Transflective type for installing the EL
H: Available in extended temperature range (operating: $-10^{\circ}C \sim +70^{\circ}C$, storage: $-40^{\circ}C \sim +80^{\circ}C$), driven by double power supply.
L: Duty = 1/16, available with single power circuit +5V.

(2) How to read the table.

○ : Underproduction.
X : Unable to produce technically.
– : Able to develop on customer's request.

Table 1 Semicustom list

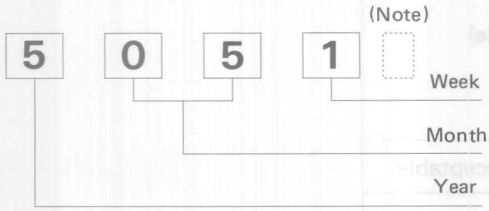
No.	Type No.	No. of display W x H	Optional specifications					Remarks
			A	T	H	LT	HT	
1	LM039	16×1	×	×	–	×	×	
2	LM054	8×1	–	○	○	×	–	
3	H2570	16×1	–	○	○	×	○	
4	LM020L	16×1	–	–	–	–	–	
5	LM015	16×1	–	○	–	×	–	
6	LM070L	20×1	–	–	–	–	–	
7	LM038	20×1	–	○	○	×	○	
8	LM027	24×1	–	○	–	×	–	
9	H2571	32×1	–	○	○	×	○	
10	LM033	32×1	–	○	–	×	–	12 o'clock type of H2571
11	H2572	40×1	○	○	○	×	–	
12	LM058	40×1	–	○	–	×	–	
13	LM016L*	16×2	○	○	○	○	○	
14	LM507L	16×2	–	–	–	–	–	12 o'clock type of LM016L
15	LM052L	16×2	–	–	–	–	–	
16	LM032L*	20×2	–	○	○	○	–	Note
17	LM060L	24×2	–	–	–	–	–	
18	LM017L*	32×2	–	○	○	○	○	
19	LM018L*	40×2	–	○	○	○	○	
20	LM035L	40×2	–	–	–	○	–	12 o'clock type of LM018L
21	LM041L*	16×4	–	–	○	○	×	Note
22	LM044L	20×4	–	–	–	○	×	Note
23	H2525	239×20	–	–	–	×	×	
24	LM021	479×24	–	–	–	×	×	
25	LM200	240×64	–	○	○	×	○	
26	LM213B	256×64	–	×	×	×	×	
27	LM212	640×48	–	–	×	×	×	
28	LM211B	480×64	–	–	×	×	×	
29	LM221B	240×128	–	–	×	×	×	
30	LM215B	480×128	–	–	×	×	×	
31	LM225S	640×200	–	–	×	×	×	
32	LM238B	240×128	–	–	×	×	×	
33	LM224B	480×128	–	–	×	×	×	
34	LM240S	480×128	–	–	×	×	×	
35	LM236S	640×200	–	–	×	×	×	
36	LM585S	640×200	–	–	×	×	×	

Note: As these LCD module do not have pad for soldering EL panel, it is necessary for the customer to solder on the mother board. Contact our office for detail.

LOT MARK

(1) Lot mark

Lot number of Hitachi LCD module is shown by four digit number as follows.



(Note) Some products have alphabet at the end.

Year mark

Year	Figure
1985	5
1986	6
1987	7
1988	8
1989	9
1990	0

Month mark

Month	Figure	Month	Figure
Jan.	01	Jul.	07
Feb.	02	Aug.	08
Mar.	03	Sept.	09
Apr.	04	Oct.	10
May	05	Nov.	11
Jun.	06	Dec.	12

Week mark

Week (Day)	Figure
21~27	1
28~ 3	2
4~10	3
11~17	4
18~20	5

(2) Location of lot mark

Indicated on the printed circuit board as below.

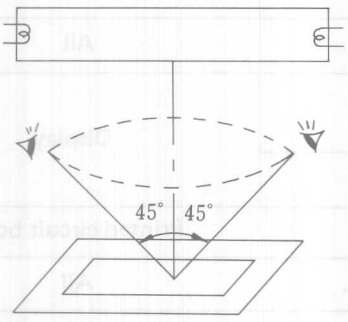
Ex.: 5051

APPEARANCE STANDARD

(1) Appearance inspection conditions

Visual inspection under single 20W fluorescent lamp with eyes to LCD distance 25 cm and lamp to LCD distance 25 to 30 cm.

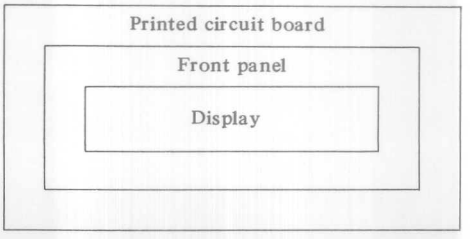
Viewing angle should be smaller than 45°.



(2) Appearance standard

No.	Items	Criteria		Applied area
1	Scratches	Distinguished one is not acceptable. (To be judged by HITACHI limit sample)		Display
2	Dents			
3	Wrinkles in polarizer			
4	Bubbles	Average dia. D (mm)	Max. number acceptable	
		1.0 < D	0	
		0.5 < D ≦ 1.0	1	
		0.3 < D ≦ 0.5	5	
		D ≦ 0.3	Ignore	
5	Stains, foreign materials	Filamentous		
		Length (mm) / Thickness (mm)	Max. number acceptable	
		Ignore / 0.02 ≧	Ignore	
		2.0 ≧ / 0.03 ≧	6	
		1.0 ≧ / 0.06 ≧	6	
		Round		
		Average dia. D (mm)	Max. number acceptable	
		D < 0.25	Ignore	
		0.25 ≦ D < 0.35	4	
		0.35 ≦ D	None	
		Those can be wiped out easily are acceptable.		All
6	Interference fringe	Distinguished one is not acceptable. (To be judged by HITACHI limit sample)		Display
7	Non-display	There should be none		
8	Chipped glass	If it has nothing to do with function, ignore.		Printed circuit board
9	Dimensions	Refer to individual acceptance specifications.		All
10	Dark spots	Average dia. D (mm)	Max. number acceptable	Display
		0 < 0.1	Ignore	
		0.1 ≦ D < 0.3	3	

Note: Definition of each area



HOW TO USE LCD MODULE

1. Liquid crystal display

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

(1) Please keep the temperature within the specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

(2) Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.).

(3) PETROLEUM BENZIN is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic substances which will be damaged by such chemicals as acetone, toluene, ethanol and isopropylalcohol.

(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.

(5) Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause deformation or color fading.

(6) Avoid contacting oil and fats.

(7) Condensation on the surface and contact terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperatures they must be warmed up in a container before coming in contact with room temperature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.

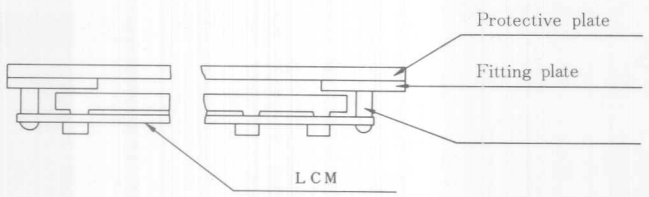
(9) Do not touch the display area with bare hands. This will stain the display area and degradate insulation between terminals. (Some cosmetics are detrimental to the polarizers).

(10) As glass is fragile, it tends to become cracked or chipped during handling especially on the edges. Please avoid dropping or jarring.

2. Liquid crystal display module

2.1 Installing LCD module

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.



(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.

(2) To prevent the module cover from being pressed, the spacers between the module and the fitting plates should be longer than 6.0 mm. (measurement tolerance: ±0.1 mm).

2.2 Precaution in handling LCD modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

(1) Do not alter, modify or change the shape of the clips on the metal frame.

(2) Do not drill attachment holes in the printed circuit board, modify its shape or change the positions of components to be attached.

(3) Do not damage or modify the pattern wiring on the printed circuit board.

(4) Absolutely do not modify or change the internal connector (conductive rubber) or touch it with another object.

(5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.

(6) Do not drop, bend or twist LCM.

2.3 Static electricity

Since this module uses a CMOS LSI, the same careful attention should be paid to static electricity as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handling LCM.

(2) Before removing LCM from its packing case or incorporating it into a set, be sure that the module and your body have the same electric potential.

(3) When soldering the terminal of LCM, make certain that the AC power source for the soldering iron does not leak.

(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced by sparks coming from the commutator of the motor.

(5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.

(6) To reduce the generation of static electricity, be careful that the air in the work is not too dried. (A relative humidity of 50% ~ 60% is recommended.)

2.4 Precaution in soldering to the LCM

(1) Observe the following when soldering lead wire, connector cable, etc., to the LCM.
- Soldering iron temperature: 280°C ±10°C
- Soldering time: 3 ~ 4 sec.
- Solder: eutectic solder

If soldering flux is used, be sure to remove any remaining flux after finishing the soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When removing the electroluminescent panel from the PC board, be sure that the solder has completely melted first. If you try to pull the components apart before the solder is completely melted, the soldered pad on the PC board could be damaged.

3. Precautions for operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (V_0)
Adjust V_0 that shows the best contrast.

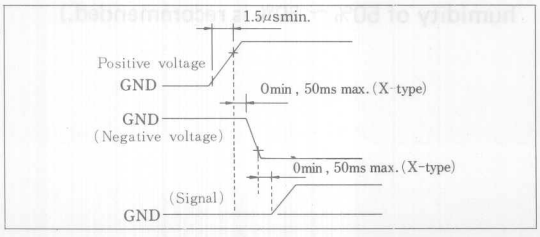
(2) Driving an LCD in the voltage above the limit shortens its life.

(3) Response time is greatly delayed at temperatures below the operating temperature range. The display area becomes dark blue at temperatures above this range. However, this does not mean the LCD will be out of order; it will recover when it returns to the specified temperature range.

(4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

(5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit.
Therefore, it must be used under the relative condition of 40°C, 50% RH.

(6) When turning on power, input each signal after the positive/negative voltage becomes stable.



4. Storage

When storing LCDs as spares for some years, the following precautions are necessary:

(1) Store them in a sealed polyethylene bag. If properly sealed, there's no need for dessicant.

(2) Store them in a dark place; do not expose to sunlight or fluorescent light. Keep the temperature between 0°C and 35°C.

(3) The polarizer surface should not come in contact with any other object. (We advise you to store them in the container in which they were shipped).

(4) Environmental conditions

(a) Humidity
Observe the following conditions both in storage and in operation.

(i) Number of dots: Below 128 x 240
Ta < 40°C . . . 95% RH or less
Ta ≧ 40°C . . . Below maximum absolute humidity of 40°C 95% RH

(ii) Number of dots: 128 x 240 or over
Ta < 40°C . . . . 85% RH or less
Ta ≧ 40°C . . . . Below maximum absolute humidity of 40°C 85% RH

(b) Exposure to high humidity and temperature

(i) Do not leave them for more than 168 hrs. at 40°C 95% RH (When number of dots is 128 x 240 or over . . . . . 40°C 85% RH)

(ii) Do not leave them for more than 168 hrs. at 60°C.

(iii) As for X-type LCM, should not be left for more than 48 hrs. at −20°C.

Note: Ta = ambient temperature

5. How to handle the electroluminescent panel

(For transflective type LCM)

5.1. Selection of electroluminescent panel

(1) The electroluminescent panel is inserted between the liquid crystal display (LCD) and printed circuit board of a liquid crystal module (LCM). Therefore, it is essential to select an electroluminescent panel that is insulated on both the PC board side and the LCD side.
It is especially important to make sure that the electroluminescent panel is insulated on the PC board side, as the wiring of the through-hole portion is exposed.

(2) It is recommended that you use an electroluminescent panel with insulated ends as shown in the diagram below. If the ends of the electroluminescent panel are exposed, a short might occur with the liquid crystal module, resulting in damage to the module.

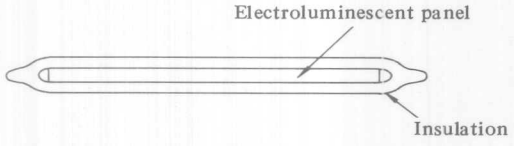


Fig. 1 Cross section of electroluminescent panel (Model not drawn to scale)

(3) Select the electroluminescent panel that is the right size for each liquid crystal module. There is a recommended size for each standard Hitachi liquid crystal module. Information on panel sizes is available upon request.

5.2 Installing the electroluminescent panel

(1) A cross section of the LCM construction is illustrated in Fig. 2. The gaps at either end through which the electroluminescent panel is inserted are made of conductive rubber (interconnectors).
When inserting the electroluminescent panel, be especially careful not to move the conductive rubber. Do not push the rubber with the edge of the panel, as the rubber might be moved from its proper position. This could damage the connection between the LCD and the PC board, resulting in a display failure.

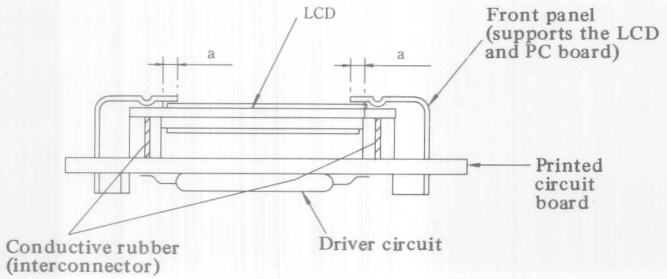


Fig. 2 Cross section of a liquid crystal module

(2) Since high voltage is applied to the feeder terminal of the electroluminescent panel, be careful to install the panel such that the feeder terminal does not touch the front panel or the PC board. (The voltage is high in comparison with that applied to the C-MOS drive circuit used in the liquid crystal module.)
If the feeder terminal is touching the front panel or PC board when the lighting voltage is applied to the panel, the drive circuit and LCD will fail. There is also the possibility that other circuits (e.g. controller on the set side, MPU, etc.) may be adversely affected by the passage of voltage through the interface.

(3) Install the electroluminescent panel such that the luminous part coincides with the window frame (effective display area) of the LCM front panel.
The distance between the window frame of the front panel and the conductive rubber (dimension a in Fig. 2) varies with each liquid crystal module, but an average is about 2.0 mm.
When determining the position where the electroluminescent panel is to be installed, be careful not to move the conductive rubber with the panel.

(4) Observe the following standards when soldering the electroluminescent panel to the PC boards.
- Soldering iron temperature: 280°C ±10°C
- Soldering time: 3 ~ 4 sec.
- Solder: eutectic solder

If soldering flux is used, be sure to remove any remaining flux after finishing the soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

(5) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering gun.

(6) When removing the electroluminescent panel from the PC board, be sure that the solder has completely melted first. If you try to pull the components apart before the solder is completely melted, the soldered pad on the PC board could be damaged.

5.3 Drive circuit of electroluminescent panel

(1) The luminance and life time of an electroluminescent panel vary depending on the drive voltage and frequency. Therefore, it is recommended that you select the drive circuit suggested by the electroluminescent panel manufacturer. Using the recommended product will assure the optimum brightness and working life of the electroluminescent panel.

6. Safety

(1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2) If any liquid leakes out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

GRAPHIC LIQUID CRYSTAL DISPLAY MODULE

This module is made of liquid crystal display device, driving LSI, printed circuit board and other parts.
By attaching controller LSI HD61830 (or HD61830B) to the module, graphic display as well as numerals, alphabets, Japanese characters and symbol display will be available.

CONTROLLER LSI HD61830 · HD61830B
CONTROL CIRCUIT BOARD
(CB1020R · CB1026R · CB1030R · CB1040R)

H2525	(239 x 20 dot)	LM225S	(640 x 200 dot)
LM021	(479 x 24 dot)	LM240S	(480 x 128 dot)
LM200	(240 x 64 dot)	LM236SB	(640 x 200 dot)
LM212	(640 x 48 dot)	LM585S	(640 x 200 dot)
LM213B	(256 x 64 dot, built-in controller)		
LM211B	(480 x 64 dot)		
LM221B	(240 x 128 dot)		
LM238B	(240 x 128 dot, built-in controller)		
LM215B	(480 x 128 dot)		
LM224B	(480 x 128 dot)		

COLOR TONE

Among graphic liquid crystal display modules, there are high-duty-ratic dynamic drive LCM that have improved in contrast and viewing angle. They are called S type and X type. Following table shows their features.

Type	Background color	Duty	Remarks
Grey	Grey	~ 1/64	Natural background color.
S	Light yellow	~ 1/128	When displayed, the color is nearly grey.
X (Developing)	Yellow	~ 1/200	It has good contrast and viewing angle, for high-duty-ratio drive over 1/100.

S type and X type have good features combining optical characteristics of the polarizer and liquid crystal materials. However, individual liquid crystal materials will be affected by the temperature causing slight change in color tone. So there are limit in temperature range, etc., for S type and X type of LCM. Ask us for detail.

CONTROLLER LSI HD61830·HD61830B

- **Graphic LCD Module Controller LSI**
- **Applied types: (1) H2525 · LM021 · LM212 · LM200 · LM211B · LM221B · LM215B/LM215SB (HD61830 is to be attached)**
  (2) LM224B · LM225S (HD61830B is to be attached)
  (3) LM213B · LM238B (HD61830 is built-in)

The HD61830 is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcomputer in the external RAM to generate dot matrix liquid crystal driving signals.
It is possible to select the graphic mode in which the 1-bit data of the external RAM corresponds to the ON/OFF state of 1 dot on liquid crystal display and the character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.
The HD61830 is produced in the CMOS process. Thus, the combination with a CMOS microcomputer can accomplish a liquid crystal display device with lower power consumption.

- **Specifications:**

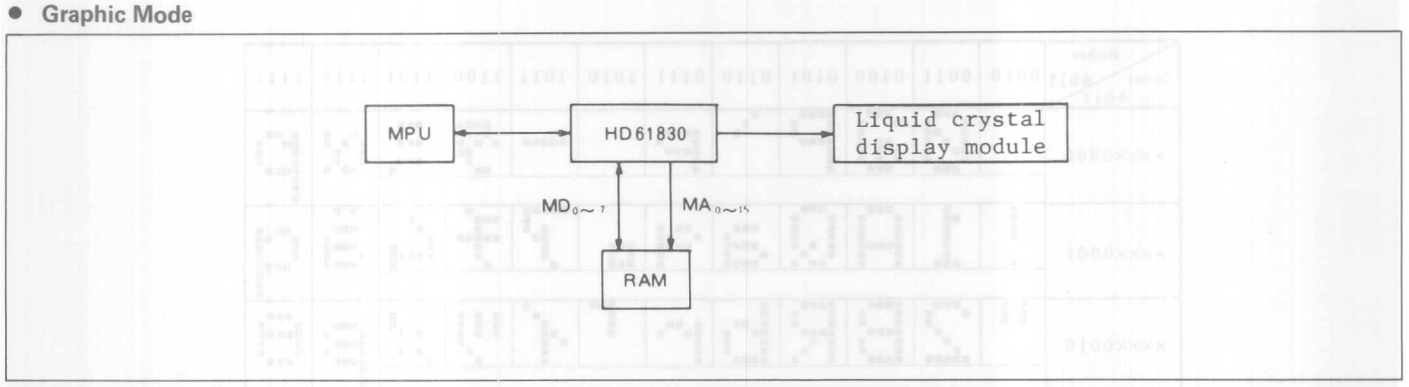
- Display control capacity
- Graphic mode — 512k dots (2^{16} bytes)
- Character mode — 4096 characters (2^{12} characters)
- Internal character generator ROM — 7360 bits
  Character fonts 5 x 7 dots 160 types
  Character fonts 5 x 10 dots 32 types
  Total 192 types
  (Can be extended to 4k byte max.)
- Interfaceable to 8-bit MPU
- Display duty (Can be selected by a program)
  Static to 1/128 duty selectable
- Various instruction functions
  Scroll, cursor ON/OFF, blink, character blink, screen clear, bit manipulation
- Display method — A or B types selectable
  (A or B: waveform)
- Internal oscillator (with external resistor and capacitor)
- Low power consumption
- Power supply: Single +5V
- CMOS process
- 60-pin flat plastic package

(Notes) HD61830B is a high speed and memory low power consumption version of HD61830. The difference between HD61830 and HD61830B are as follows;
(1) Internal oscillation circuit
(2) Additional memory control signals
(3) Connection method in master/slave mode
If you need detailed information, please refer to "Hitachi MOS LSI data book LCD driver LSI" or contact following office.
Semiconductor & Integrated Circuit Div.
New Marunouchi Bldg., 5-1 Marunouchi 1 chome, Chiyoda-ku, Tokyo 100, Tel: Tokyo (03) 212-1111

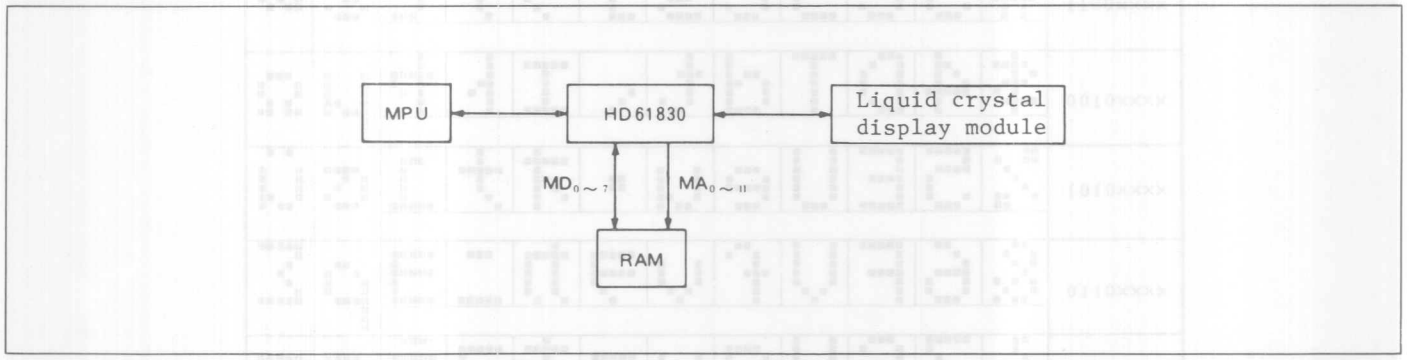
■ INTERNAL CHARACTER GENERATOR PATTERNS AND CHARACTER CODES

■ EXAMPLE OF CONFIGURATION

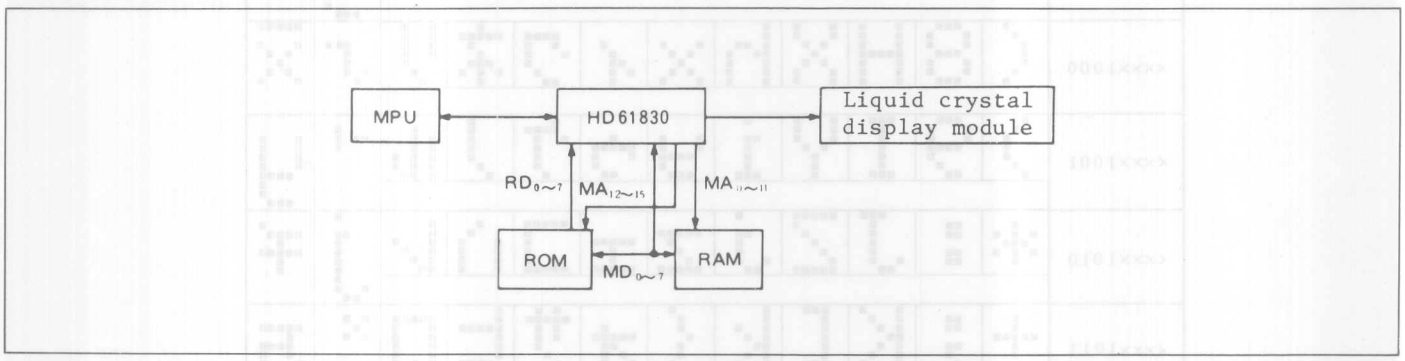
- **Graphic Mode**



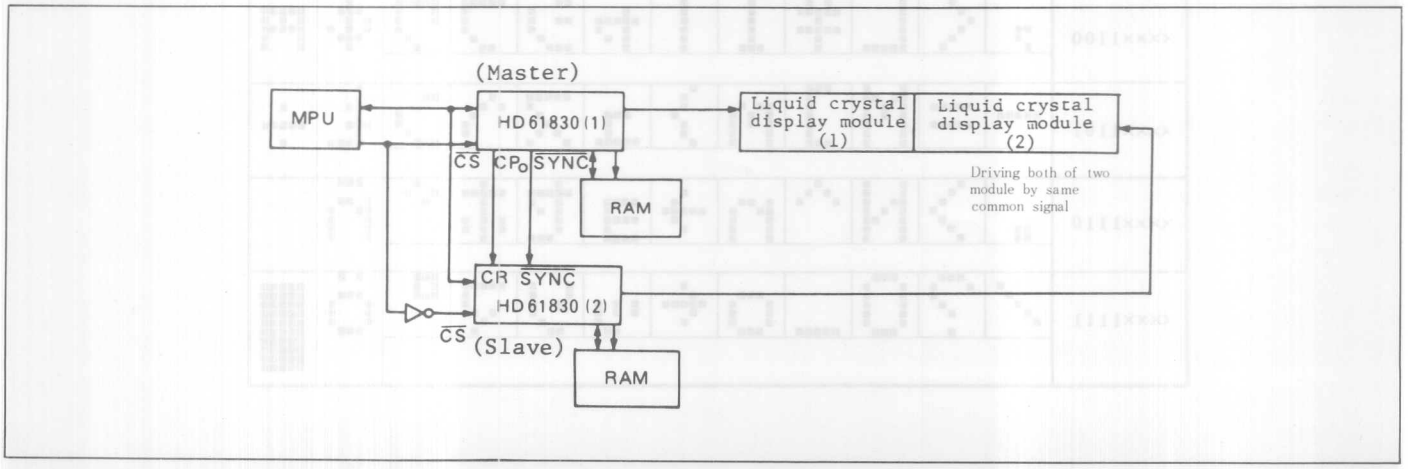
- **Character Mode (1) (Internal Character Generator)**



- **Character Mode (2) (External Character Generator)**

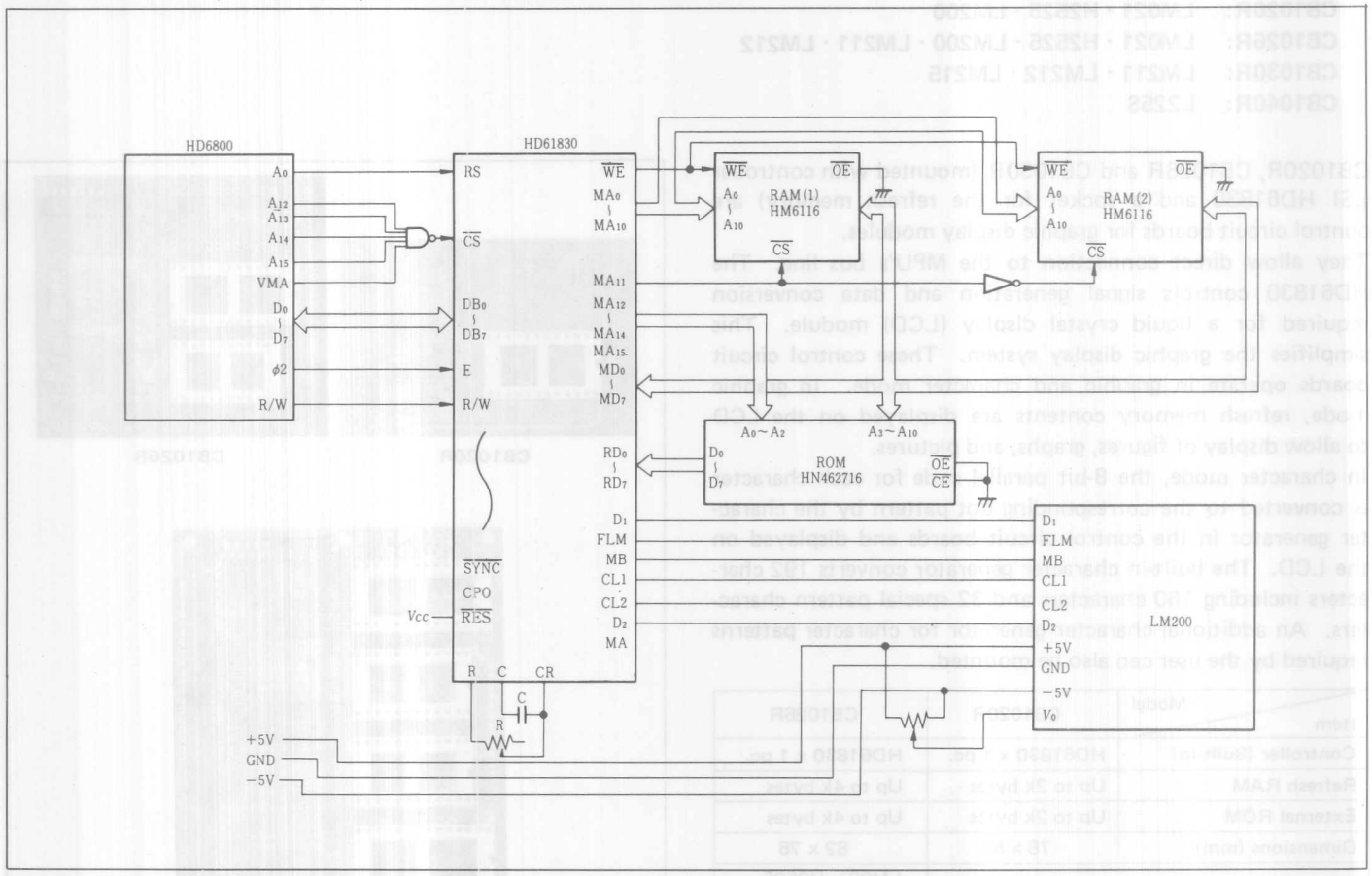


- **Parallel Operation**

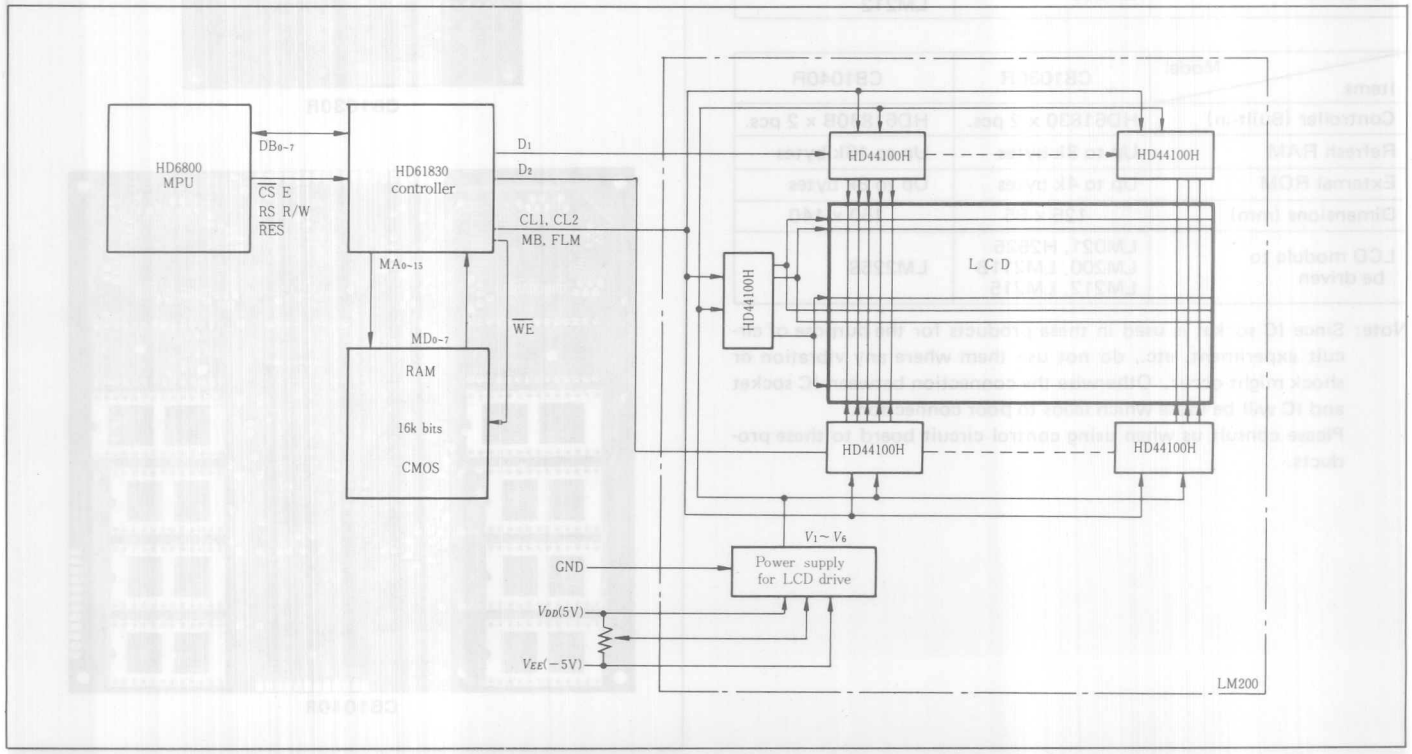


■ APPLICATION

1. Character mode, External CG, Character Font 8 x 8



2. Graphic mode



CONTROL CIRCIT BOARD CB1020R, CB1026R, CB1030R, CB1040R

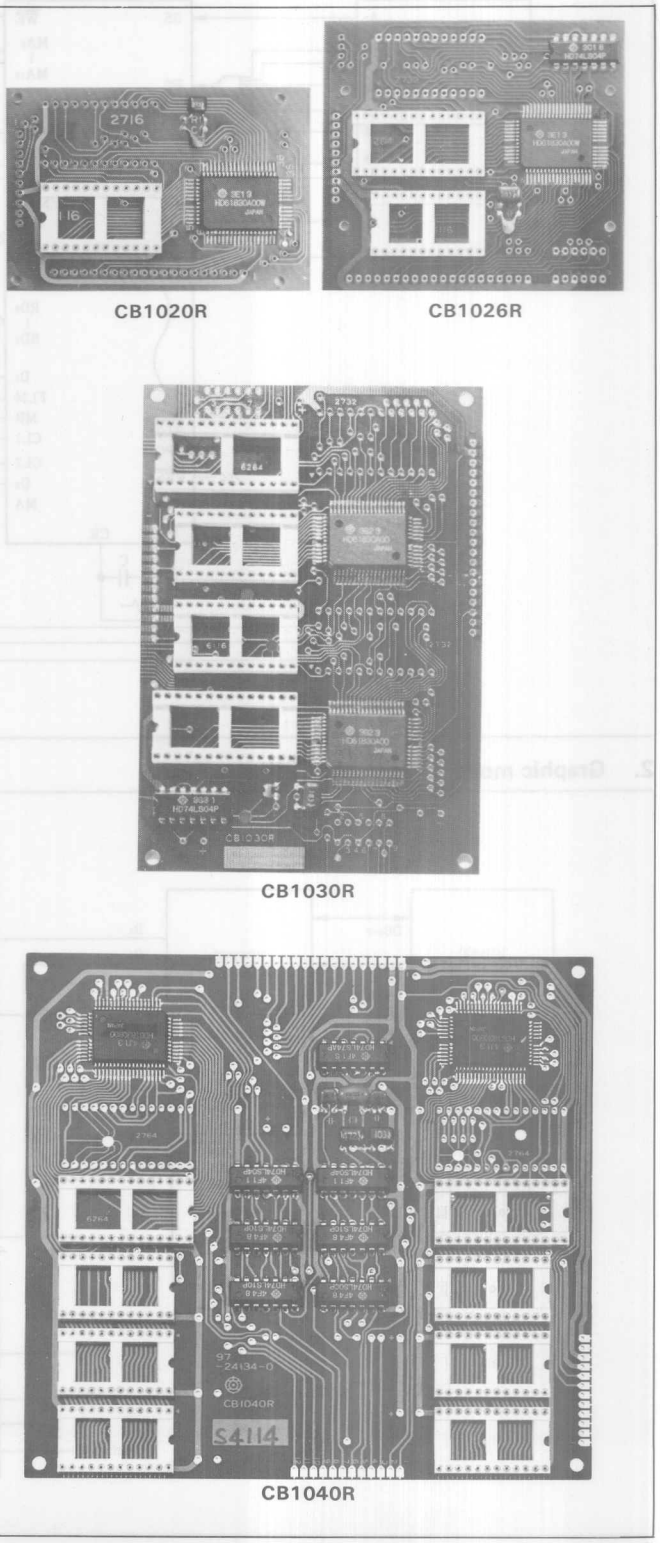
- **BUILT-IN CONTROLLER LSI HD61830**
- **Applied types: Control circuit board can be applied to following types.**
  CB1020R: LM021 · H2525 · LM200
  CB1026R: LM021 · H2525 · LM200 · LM211 · LM212
  CB1030R: LM211 · LM212 · LM215
  CB1040R: L225S

CB1020R, CB1026R and CB1030R (mounted with controller LSI HD61830 and a socket for the refresh memory) are control circuit boards for graphic display modules.
They allow direct connection to the MPU's bus line. The HD61830 controls signal generation and data conversion required for a liquid crystal display (LCD) module. This simplifies the graphic display system. These control circuit boards operate in graphic and character mode. In graphic mode, refresh memory contents are displayed on the LCD to allow display of figures, graphs, and pictures.
In character mode, the 8-bit parallel code for each character is converted to the corresponding dot pattern by the character generator in the control circuit boards and displayed on the LCD. The built-in character generator converts 192 characters including 160 characters and 32 special pattern characters. An additional character generator for character patterns required by the user can also be mounted.

Item \ Model	CB1020R	CB1026R
Controller (Built-in)	HD61830 x 1 pc.	HD61830 x 1 pc.
Refresh RAM	Up to 2k bytes	Up to 4k bytes
External ROM	Up to 2k bytes	Up to 4k bytes
Dimensions (mm)	78 x 53	82 x 76
LCD module to be driven	LM021, H2525 LM200	LM021, H2525, LM200, LM211B LM212

Items \ Model	CB1030R	CB1040R
Controller (Built-in)	HD61830 x 2 pcs.	HD61830B x 2 pcs.
Refresh RAM	Up to 8k bytes	Up to 16k bytes
External ROM	Up to 4k bytes	Up to 8k bytes
Dimensions (mm)	125 x 85	150 x 140
LCD module to be driven	LM021, H2525 LM200, LM211B LM212, LM215	LM225S

Note: Since IC socket is used in these products for the purpose of circuit experiment, etc., do not use them where any vibration or shock might occur. Otherwise the connection between IC socket and IC will be loose which leads to poor connection.
Please consult us when using control circuit board to these products.



CB1020R CB1026R

CB1030R

CB1040R

H2525

- 239dot (W) x 20 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see page 20).

MECHANICAL DATA (Nominal dimensions)

Module size	220W x 53H x 15T (max.) mm
Effective display area	163W x 17H mm
Number of dots	239W x 20H dot
Dot size	0.55W x 0.55H mm
Dot pitch	0.65W x 0.65H mm
Weight	about 100g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD}V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V, V_{EE}=−5.0V±0.25V

Input "high" voltage (V_{iH})	0.7 x V_{DD}V min.
Input "low" voltage (V_{iL})	0.3 x V_{DD}V max.
Clock frequency (f_{CL2})	210 kHz min.
	300 kHz typ.
	390 kHz max.
Power supply current (I_{DD})	3mA typ.
(I_{EE})	1 mA typ.

(D_1, D_2 = GND, f_{CL2} = 300 kHz)

Power supply for LCD drive (Recommended) (V_O-V_{EE})

Duty = 1/20

Ta= 0°C	5.5V typ.
Ta=25°C	5.0V typ.
Ta=50°C	4.0V typ.

OPTICAL DATA ..... See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	FLM	H	The FLM single indicates the begining of each display cycle.
2	M	H/L	Control signal for a.c. driving
3	CL1	H→L	The CL1 latches the serial data in the shift registers.
4	D1	H/L	Serial row data
5	CL2	H→L	Clock signal for shifting the serial data
6	V_{DD}(+5V)	–	Power supply for logic circuit
7	V_{SS}(GND)	–	Ground
8	V_{EE}(−5V)	–	Power supply for LC driving
9	V_O	–	Operating voltage for LC driving
10	NC	–	No connection

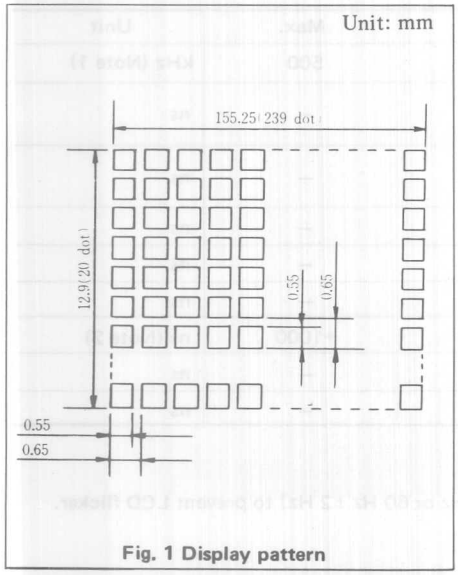


Fig. 1 Display pattern

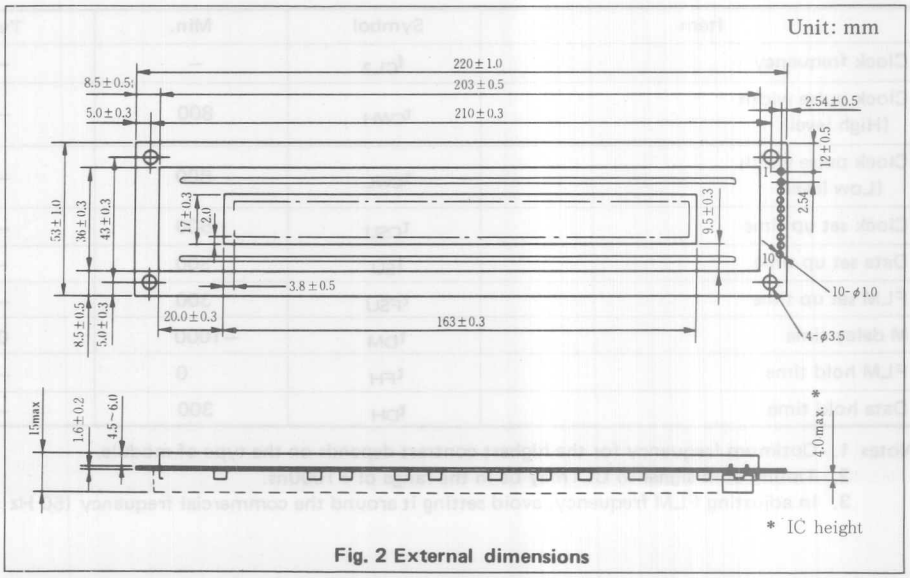


Fig. 2 External dimensions

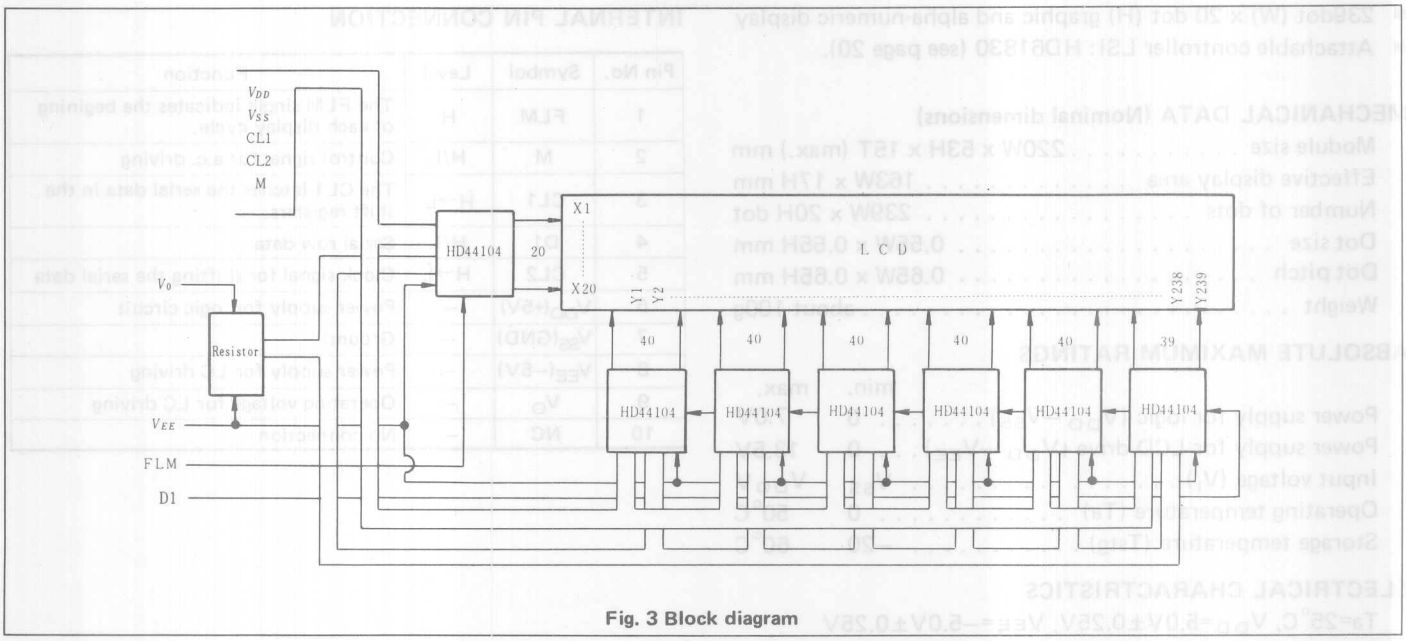
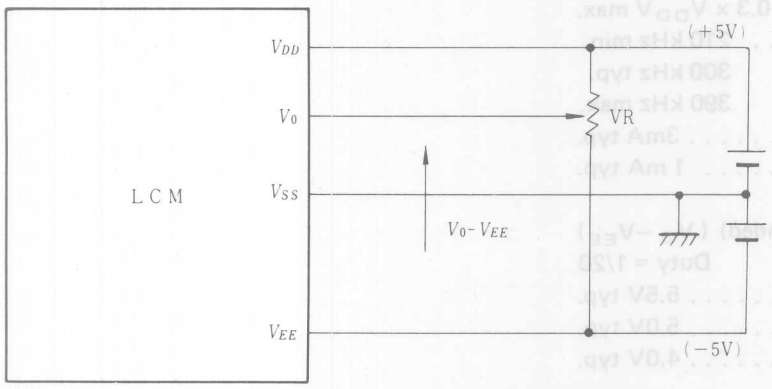


Fig. 3 Block diagram



V_O-V_{EE}: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CL2}	–	–	500	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	800	–	–	ns
Clock pulse width (Low level)	t_{CWL}	800	–	–	ns
Clock set up time	t_{CSU}	500	–	–	ns
Data set up time	t_{SU}	300	–	–	ns
FLM set up time	t_{FSU}	300	–	–	ns
M delay time	t_{DM}	−1000	0	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	300	–	–	ns

Notes 1. Optimum frequency for the highest contrast depends on the type of module.
2. Timing of M signal to CL1may be in the range of ±1000ns.
3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ±2 Hz or 60 Hz ±2 Hz) to prevent LCD flicker.

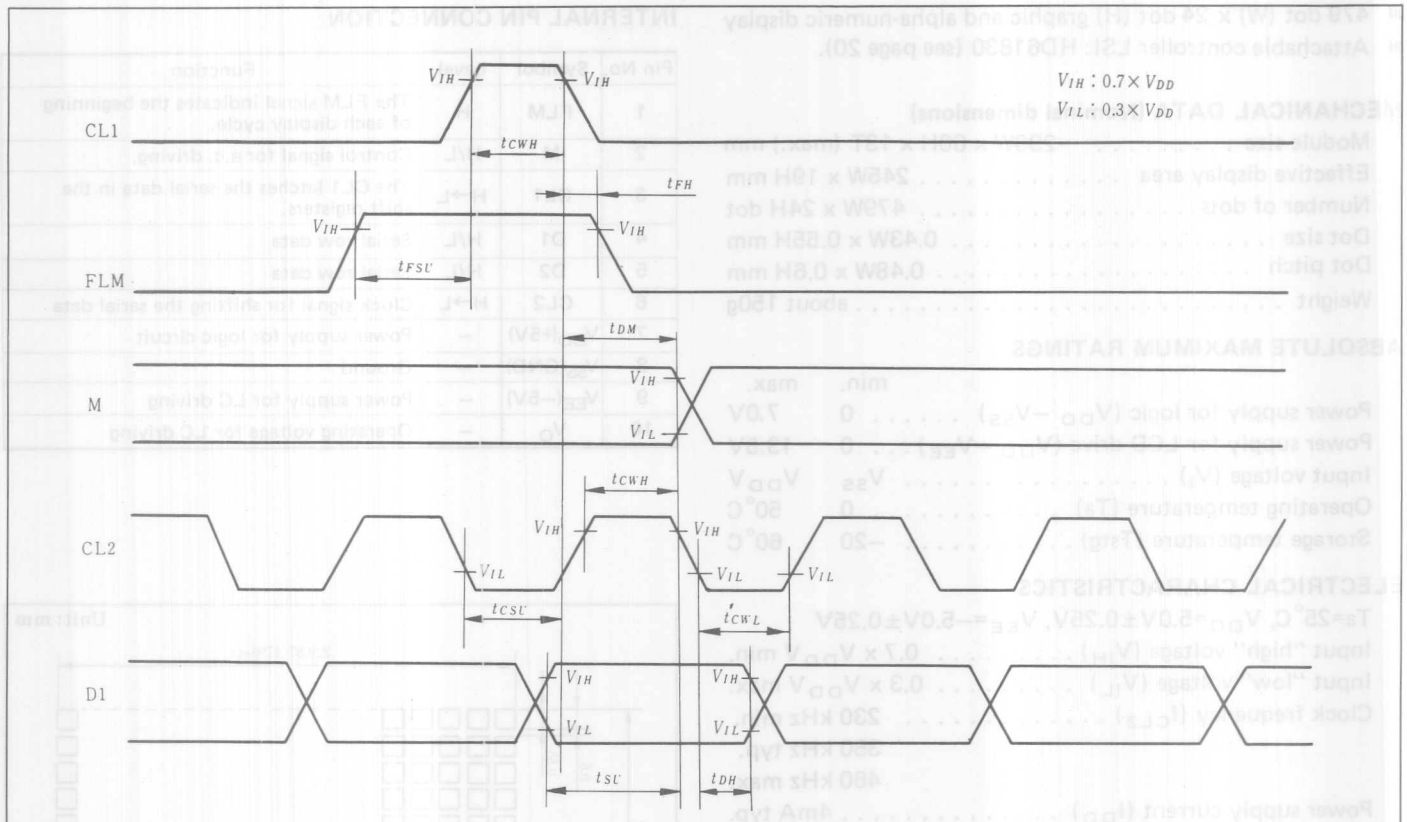


Fig. 5 Interface timing (data write)

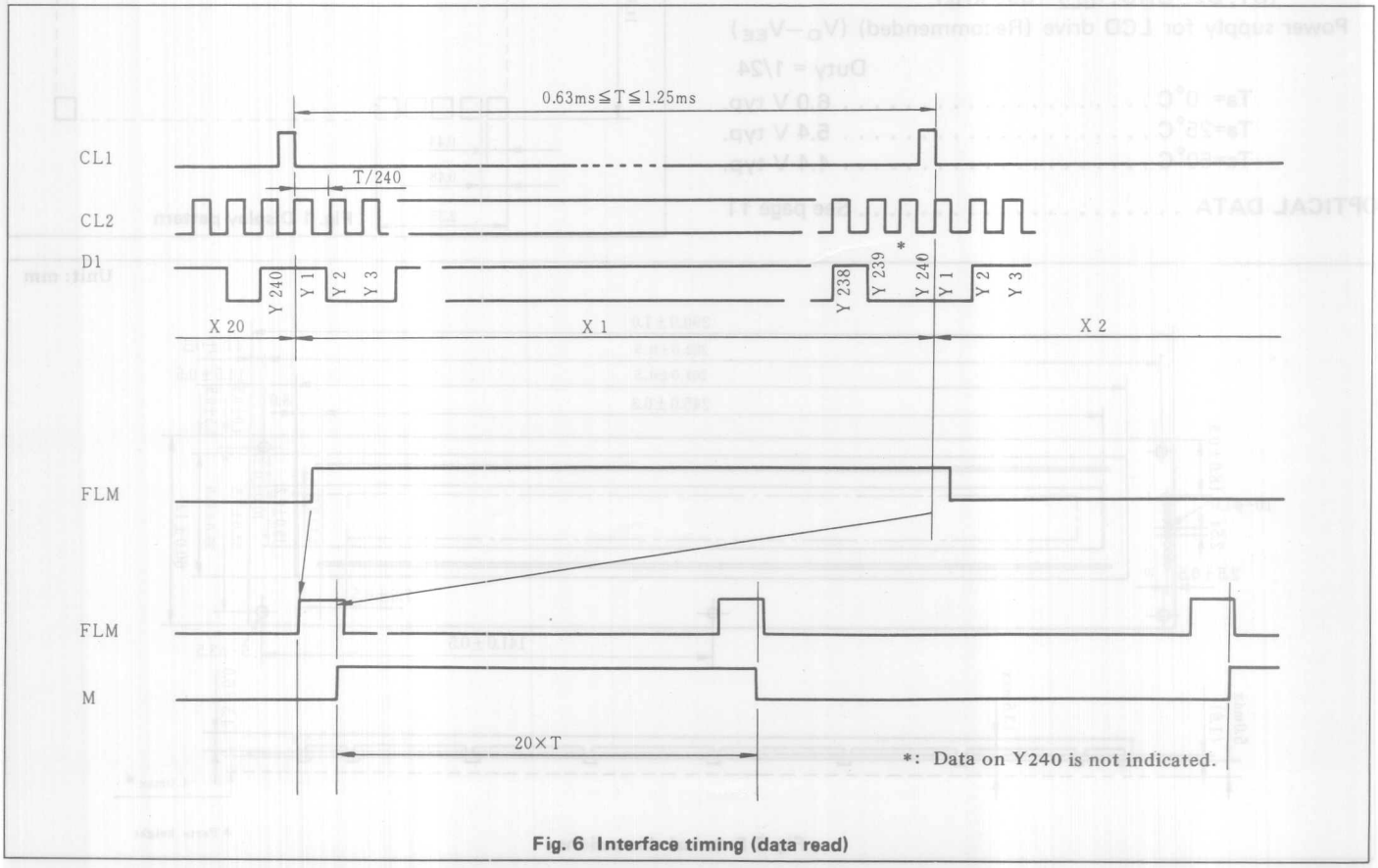


Fig. 6 Interface timing (data read)

LM021

- 479 dot (W) x 24 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see page 20).

MECHANICAL DATA (Nominal dimensions)

Module size	290W x 60H x 13T (max.) mm
Effective display area	245W x 19H mm
Number of dots	479W x 24H dot
Dot size	0.43W x 0.55H mm
Dot pitch	0.48W x 0.6H mm
Weight	about 150g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD}V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V, V_{EE}=−5.0V±0.25V

Input "high" voltage (V_{iH})	0.7 x V_{DD}V min.
Input "low" voltage (V_{iL})	0.3 x V_{DD}V max.
Clock frequency (f_{CL2})	230 kHz min.
	350 kHz typ.
	460 kHz max.
Power supply current (I_{DD})	4mA typ.
(I_{EE})	2mA typ.

(D_1, D_2=GND, f_{CL2}=350 kHz)

Power supply for LCD drive (Recommended) (V_O-V_{EE})

Duty = 1/24

Ta= 0°C	6.0 V typ.
Ta=25°C	5.4 V typ.
Ta=50°C	4.4 V typ.

OPTICAL DATA See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	FLM	H	The FLM signal indicates the beginning of each display cycle.
2	M	H/L	Control signal for a.c. driving.
3	CL1	H→L	The CL1 latches the serial data in the shift registers.
4	D1	H/L	Serial row data
5	D2	H/L	Serial row data
6	CL2	H→L	Clock signal for shifting the serial data
7	V_{DD}(+5V)	–	Power supply for logic circuit
8	V_{SS}(GND)	–	Ground
9	V_{EE}(−5V)	–	Power supply for LC driving
10	V_O	–	Operating voltage for LC driving

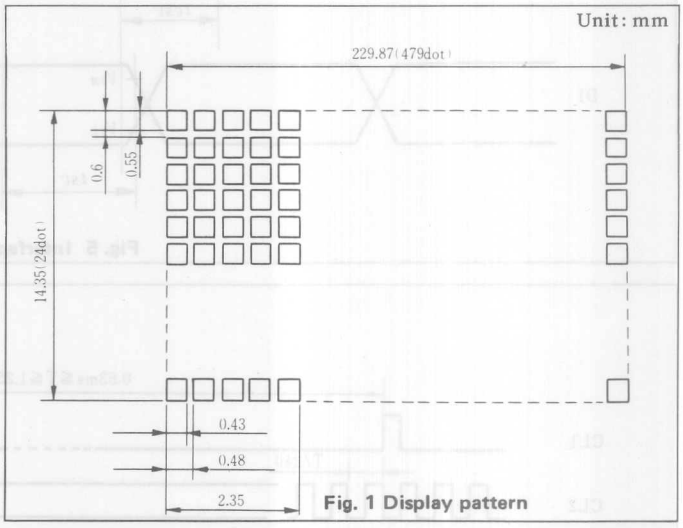


Fig. 1 Display pattern

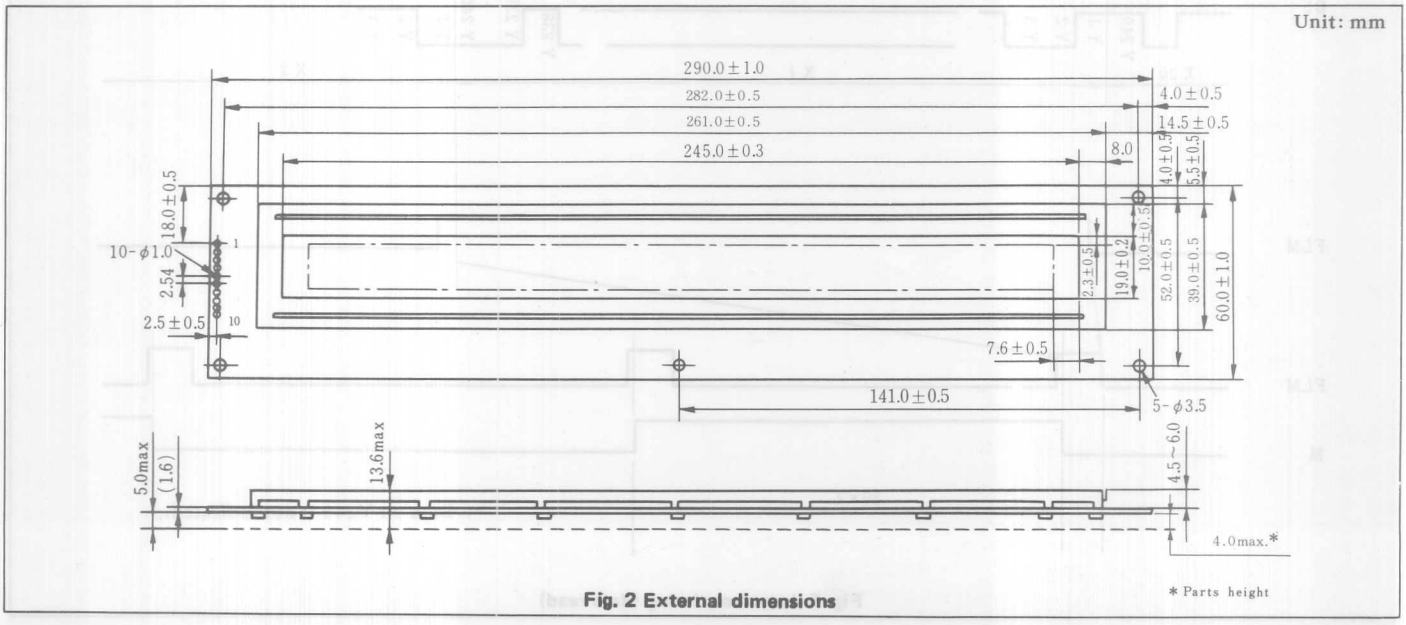
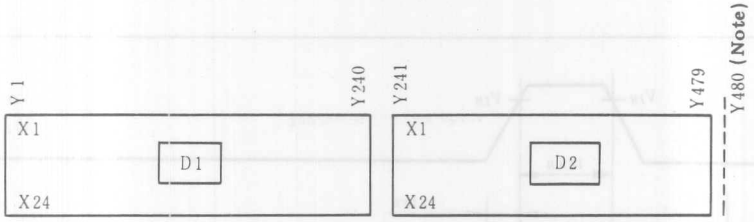


Fig. 2 External dimensions

HITACHI



Note: Y480 is a dummy line.

Fig. 3 Correspondence of display with data

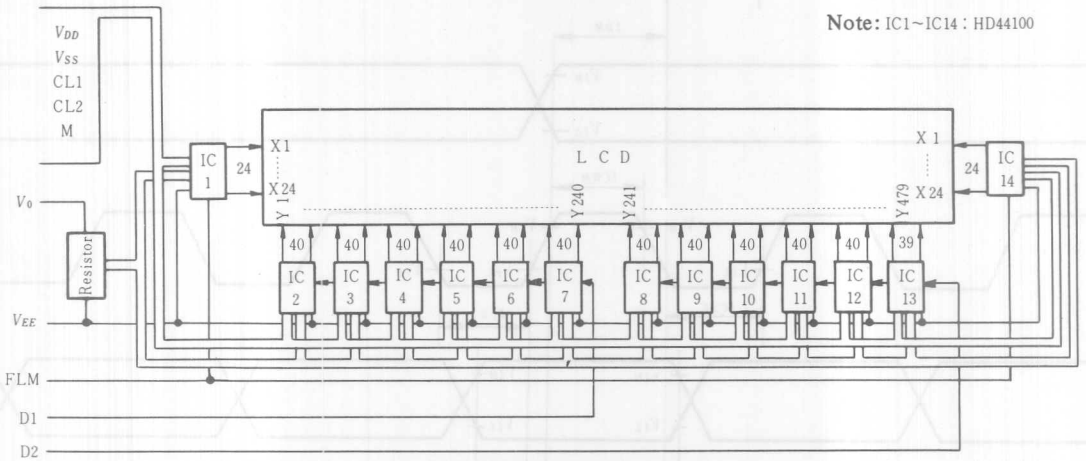
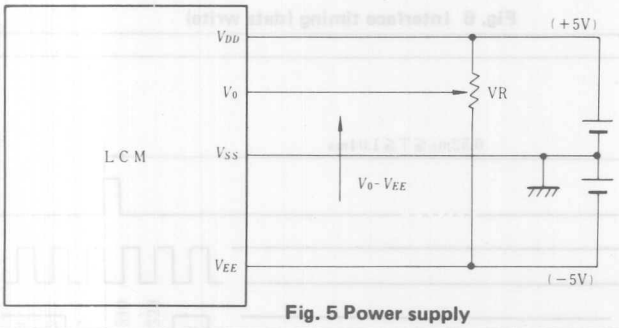


Fig. 4 Block diagram



V_O-V_{EE}: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 5 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CL2}	–	–	500	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	800	–	–	ns
Clock pulse width (Low level)	t_{CWL}	800	–	–	ns
Clock set up time	t_{CSU}	500	–	–	ns
Data set up time	t_{SU}	300	–	–	ns
FLM set up time	t_{FSU}	300	–	–	ns
M delay time	t_{DM}	−1000	0	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	300	–	–	ns

Notes 1. Optimum frequency for the highest contrast depends on the type of module.
2. Timing of M signal to CL1may be in the range of ±1000ns.
3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ±2 Hz or 60 Hz ±2 Hz) to prevent LCD flicker.

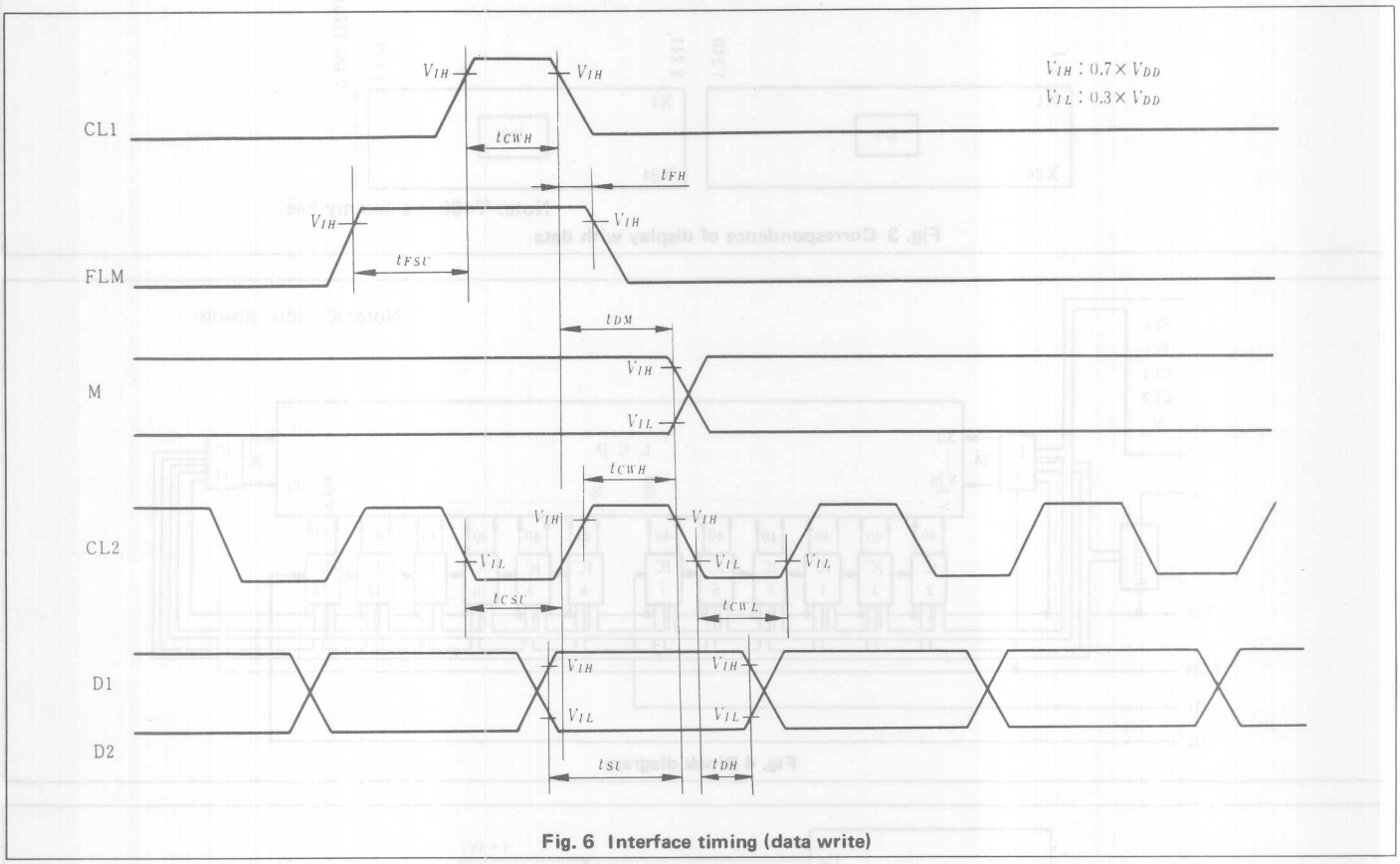


Fig. 6 Interface timing (data write)

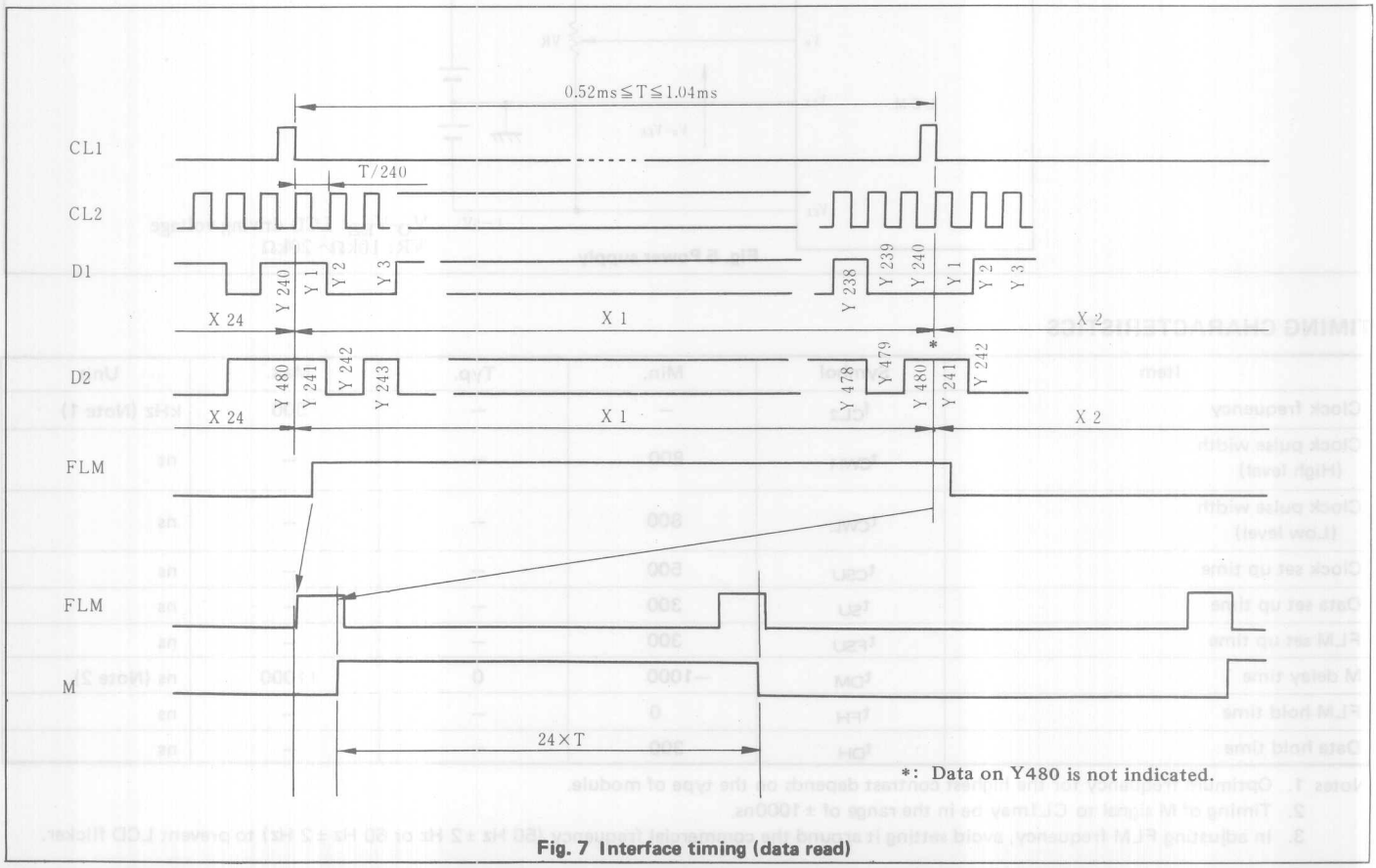


Fig. 7 Interface timing (data read)

LM212

- 640 dot(W) x 48 dot(H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see page 20).

OPTICAL DATA . . . . . See page 11

MECHANICAL DATA (Nominal dimensions)

Module size	270W x 63H x 13.8T (max.) mm
Effective display area	241W x 25H mm
Number of dots	640W x 48H dot
Dot size	0.32W x 0.38H mm
Dot pitch	0.37W x 0.43H mm
Weight	about 175 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	15.0 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V, V_{EE} = −9V

(Internal power supply)

	min.	max.
Input "high" voltage (Vi_H)	3.5	V_{DD}V
Input "low" voltage (Vi_L)	0	1.5 V max.

Clock frequency (f_{CL2}) . . . . . 1,075 kHz min.
1,152 kHz typ.
1,228 kHz max.

Power supply current (I_{DD}) . . . . . 10 mA typ.
(D_1, D_2 = GND, f_{CL2} = 1,152 kHz)

Power supply for LCD drive (Recommended) ($V_{DD} - V_O$)
Duty = 1/48

Ta = 0°C	12.5 V typ.
Ta = 25°C	11.0 V typ.
Ta = 40°C	9.7 V typ.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data (left half)
2	FLM	H	The FLM signal indicates the beginning of each display cycle
3	M	H/L	Control signal for AC driving
4	CL1	H→L	The CL1 latches the serial data in the shift registers
5	CL2	H→L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data (right half)
7	V_{DD}(+5V)	–	Power supply for logic circuit
8	V_{SS}	–	Ground
9	V_{EE}(−10V)	–	Power supply for LC driving
10	V_O	–	Operating voltage for LC driving

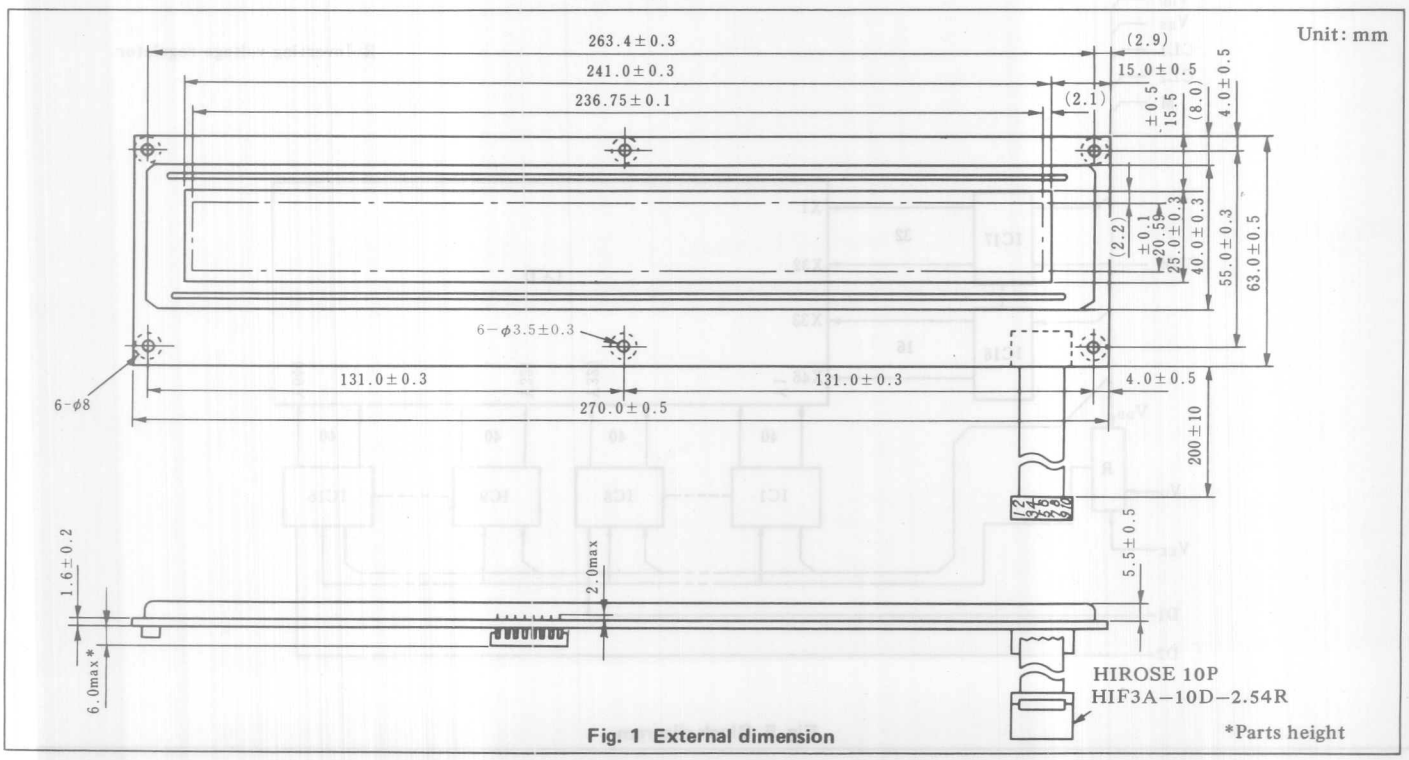


Fig. 1 External dimension

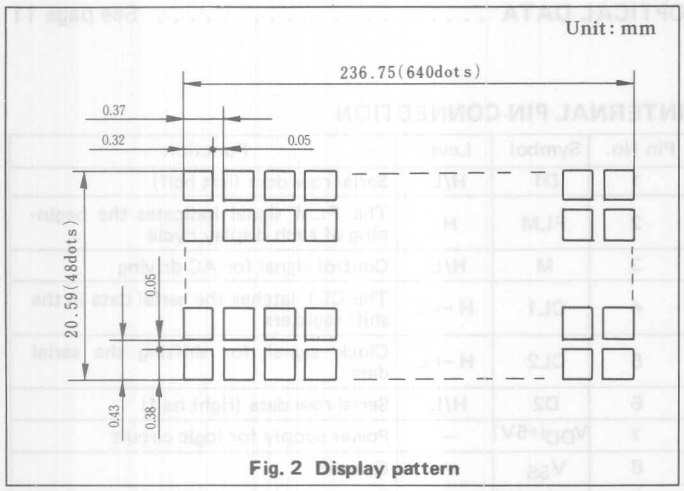


Fig. 2 Display pattern

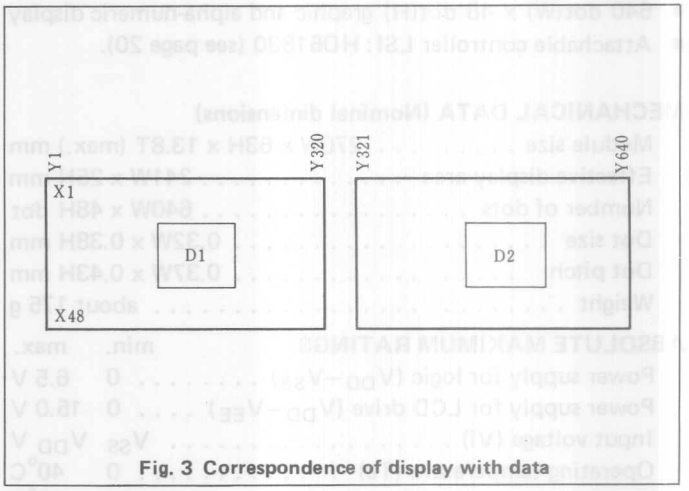
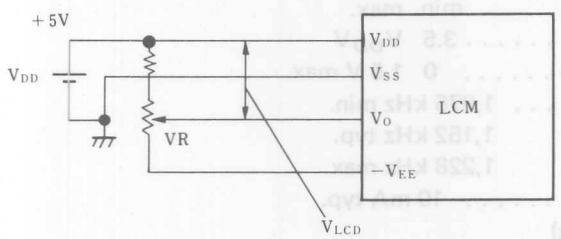
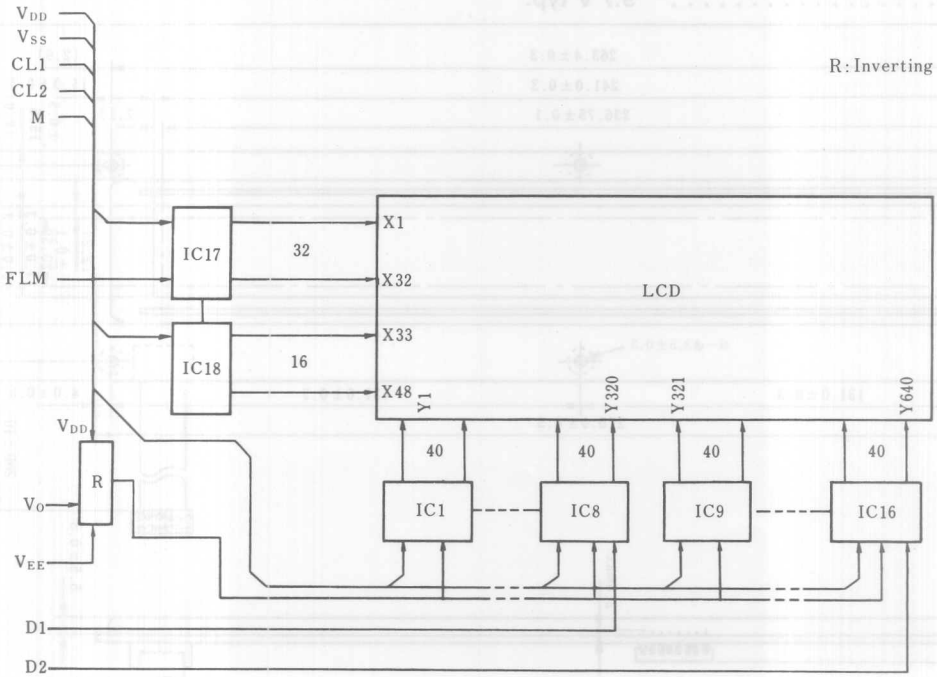


Fig. 3 Correspondence of display with data



R: 30 ~ 50kΩ
VR: 20kΩ
V_{LCD}: Operating voltage for LC driving

Fig. 4 Power supply



R: Inverting voltage regulator

Fig. 5 Block diagram

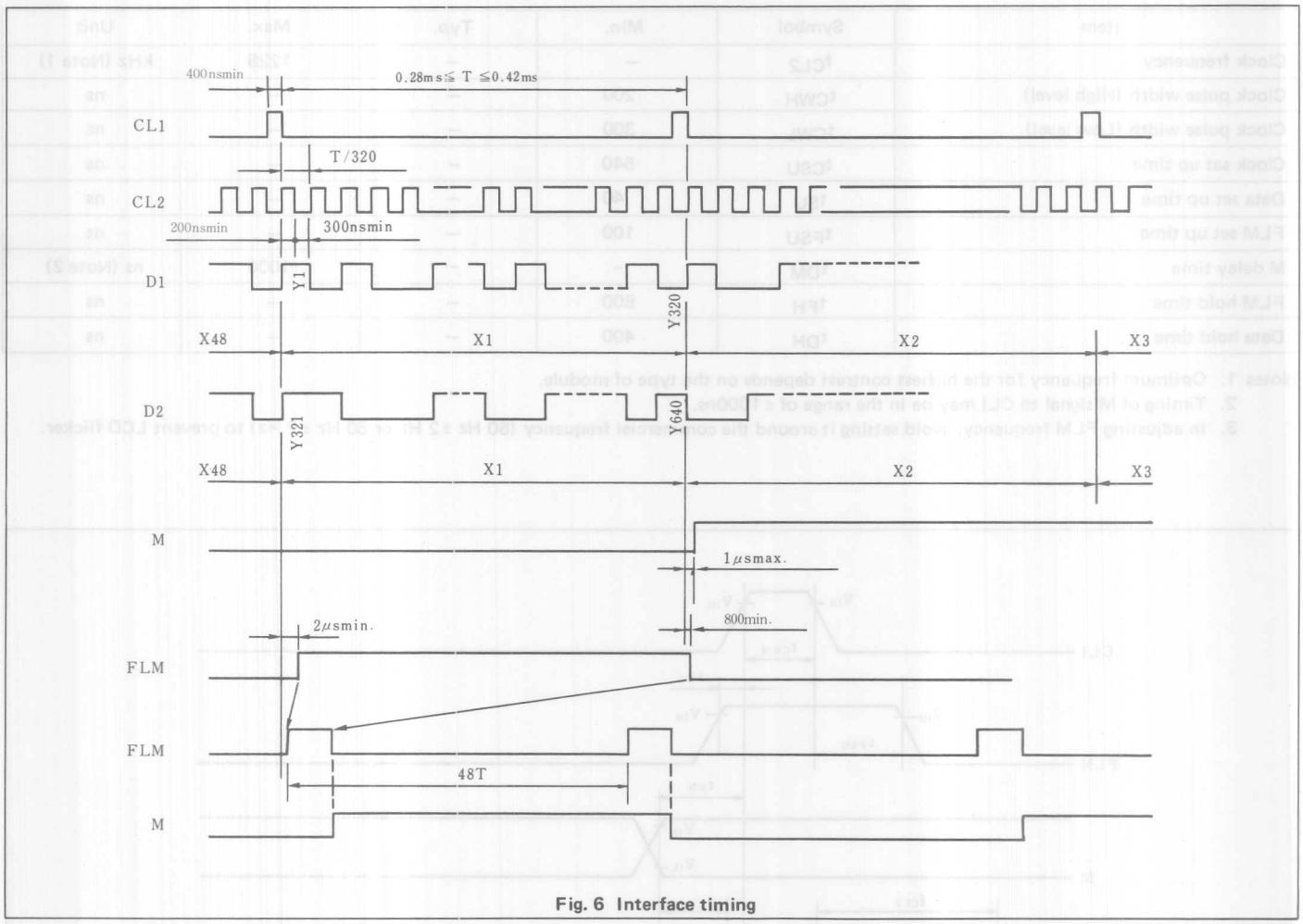


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CL2}	–	–	1228	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	200	–	–	ns
Clock pulse width (Low level)	t_{CWL}	300	–	–	ns
Clock set up time	t_{CSU}	540	–	–	ns
Data set up time	t_{SU}	40	–	–	ns
FLM set up time	t_{FSU}	100	–	–	ns
M delay time	t_{DM}	–	–	+1000	ns (Note 2)
FLM hold time	t_{FH}	800	–	–	ns
Data hold time	t_{DH}	400	–	–	ns

Notes 1. Optimum frequency for the highest contrast depends on the type of module.
2. Timing of M signal to CLI may be in the range of ±1000ns.
3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ±2 Hz or 60 Hz ±2 Hz) to prevent LCD flicker.

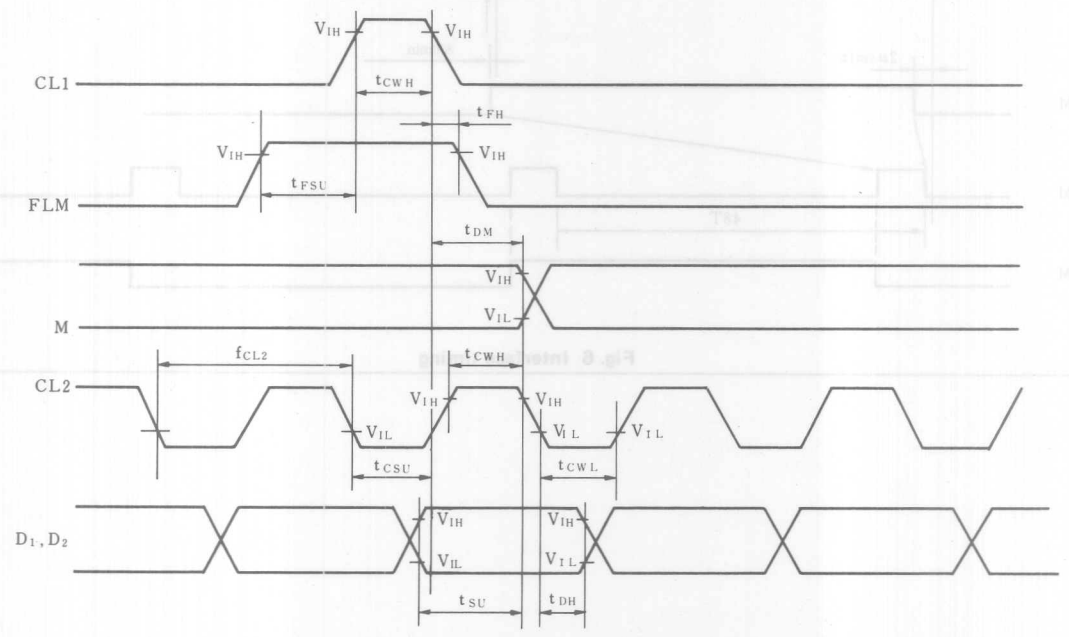


Fig. 7 Interface timing

LM200

- 240 dot (W) x 64 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see page 20).

MECHANICAL DATA (Nominal dimensions)

Module size	180W x 75H x 13.8T (max.) mm
Effective display area	132W x 39H mm
Number of dots	240W x 64H dot
Dot size	0.48W x 0.48H mm
Dot pitch	0.53W x 0.53H mm
Weight	about 150g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD}V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V, V_{EE}=−5.0V±0.25V

Input "high" voltage (V_{iH})	0.7 x V_{DD}V min.
Input "low" voltage (V_{iL})	0.3 x V_{DD}Vmax.
Clock frequency (f_{CL2})	390 kHz min.
	460 kHz typ.
	520 kHz max.
Power supply current (I_{DD})	5mA typ.
(D_1, D_2=GND, f_{CL2}=460 kHz)	
Power supply for LCD drive (Recommended) (V_O-V_{EE})	
	Duty = 1/32
Ta= 0°C	8.1 V typ.
Ta=25°C	7.4 V typ.
Ta=50°C	6.5 V typ.

OPTICAL DATA ..... See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data
2	FLM	H	The FLM signal indicates the beginning of each display cycle.
3	M	H/L	Control signal for a.c. driving
4	CL1	H→L	The CL1 latches the serial data in the shift registers.
5	CL2	H→L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data
7	V_{DD}(+5V)		Power supply for logic circuit
8	V_{SS}(GND)	–	Ground
9	V_{EE}(−5V)	–	Power supply for LC driving
10	V_O	–	Operating voltage for LC driving

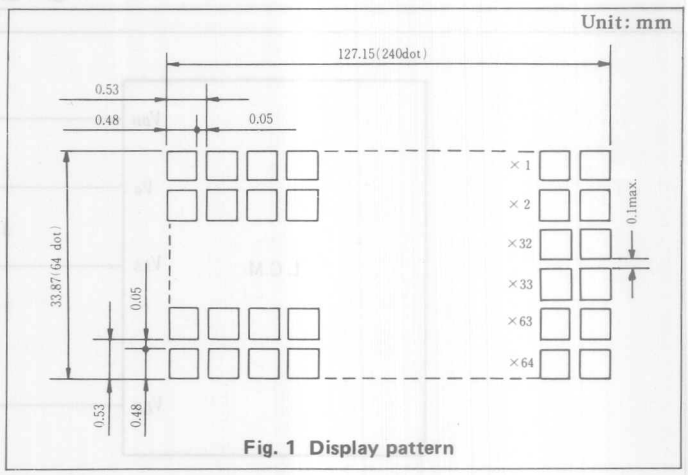


Fig. 1 Display pattern

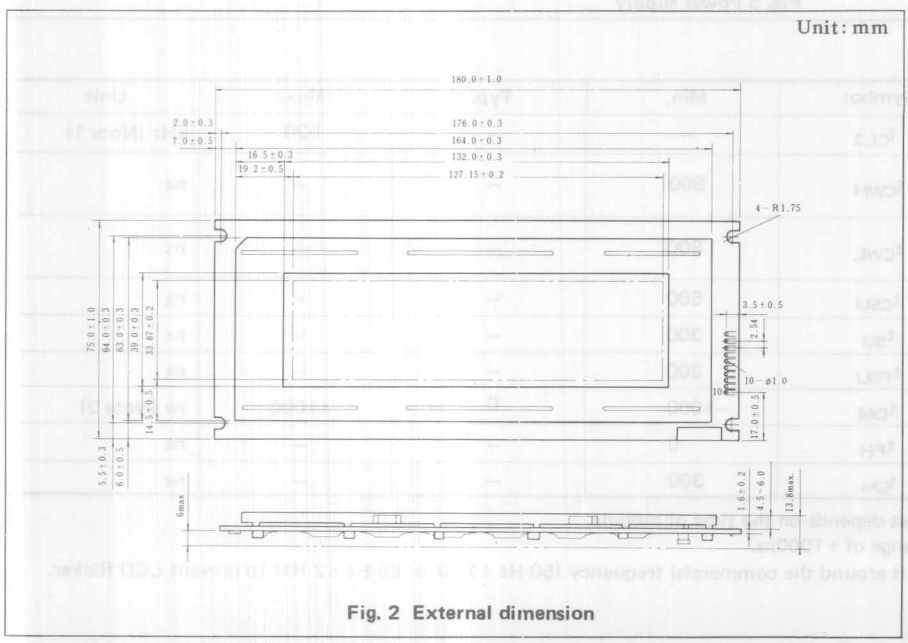


Fig. 2 External dimension

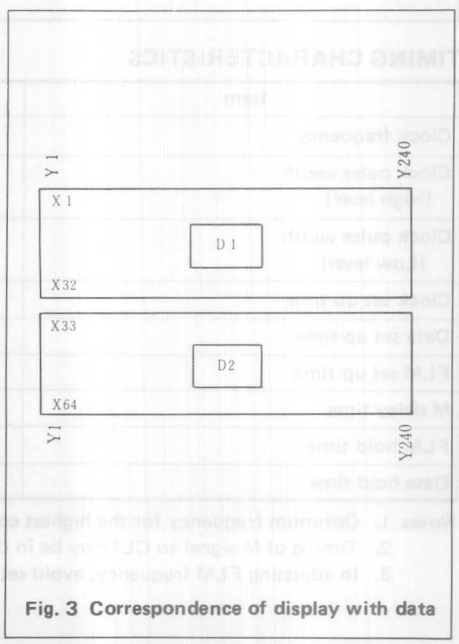


Fig. 3 Correspondence of display with data

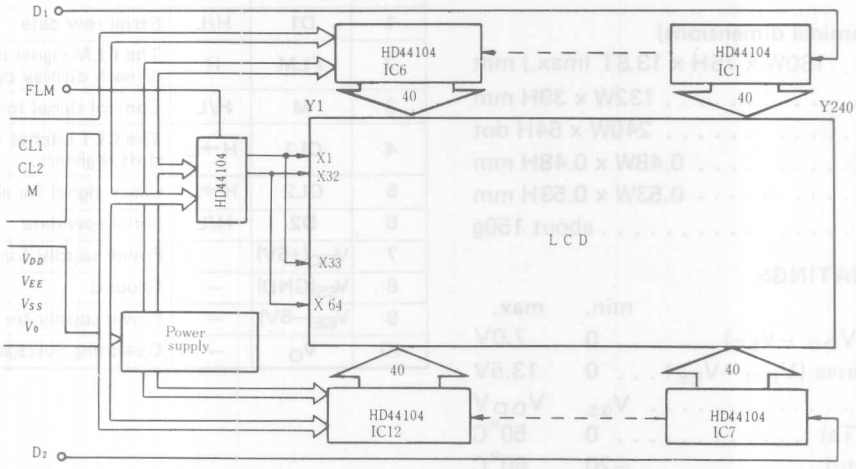
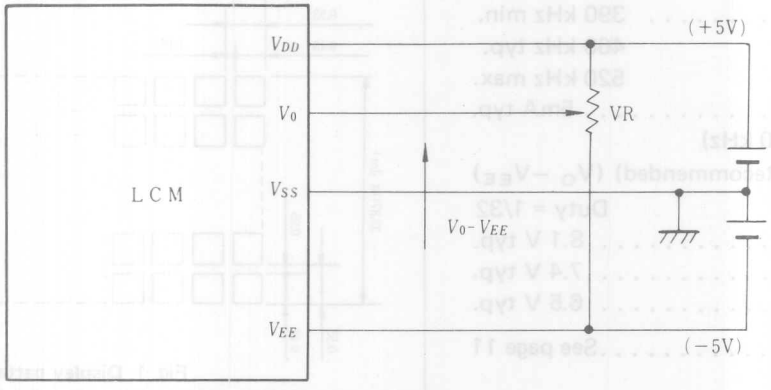


Fig. 4 Block diagram



V_O-V_{EE}: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 5 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CL2}	–	–	520	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	800	–	–	ns
Clock pulse width (Low level)	t_{CWL}	800	–	–	ns
Clock set up time	t_{CSU}	500	–	–	ns
Data set up time	t_{SU}	300	–	–	ns
FLM set up time	t_{FSU}	300	–	–	ns
M delay time	t_{DM}	−1000	0	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	300	–	–	ns

Notes 1. Optimum frequency for the highest contrast depends on the type of module.
2. Timing of M signal to CL1may be in the range of ±1000ns.
3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ±2 Hz or 60 Hz ±2 Hz) to prevent LCD flicker.

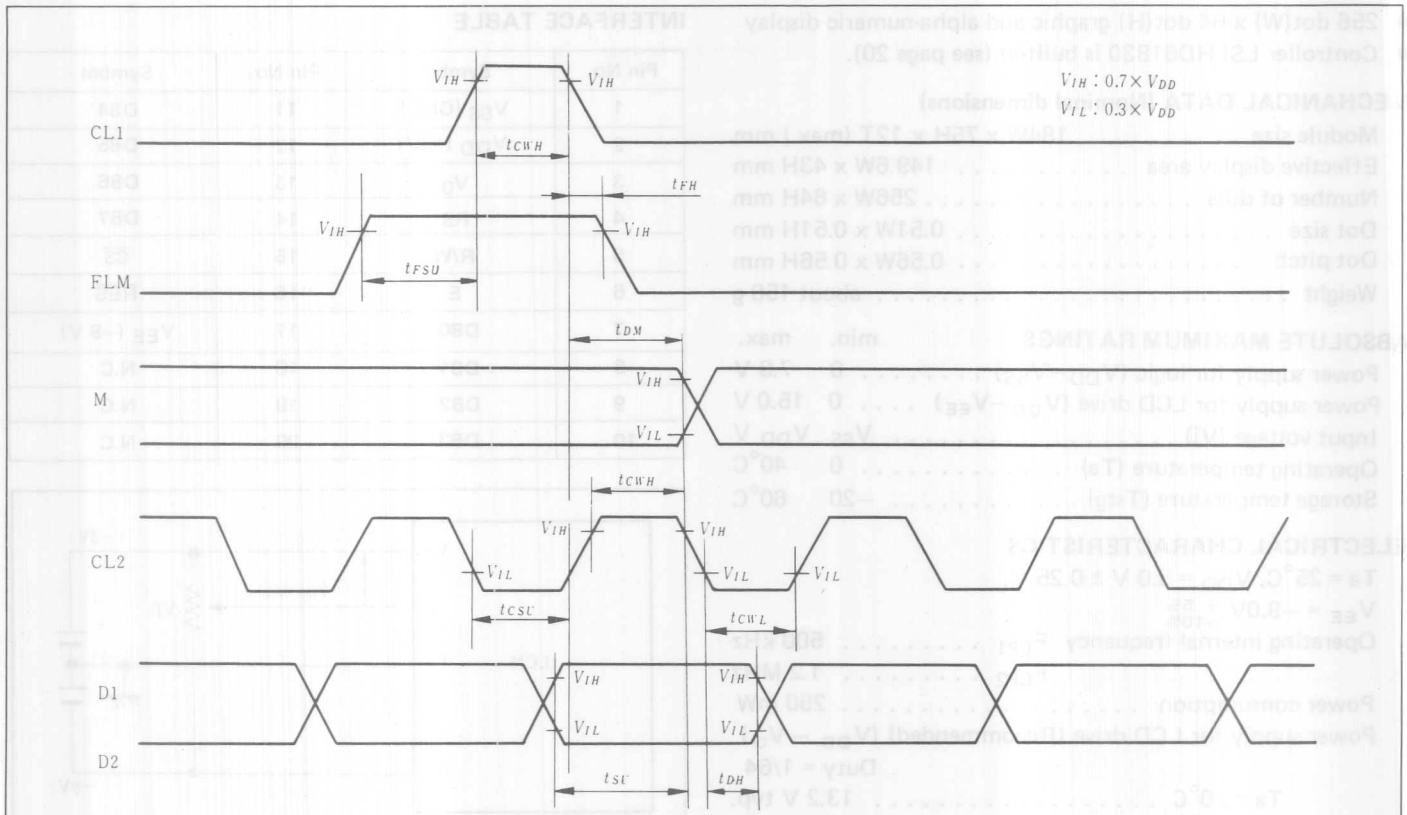


Fig. 6 Interface timing (data write)

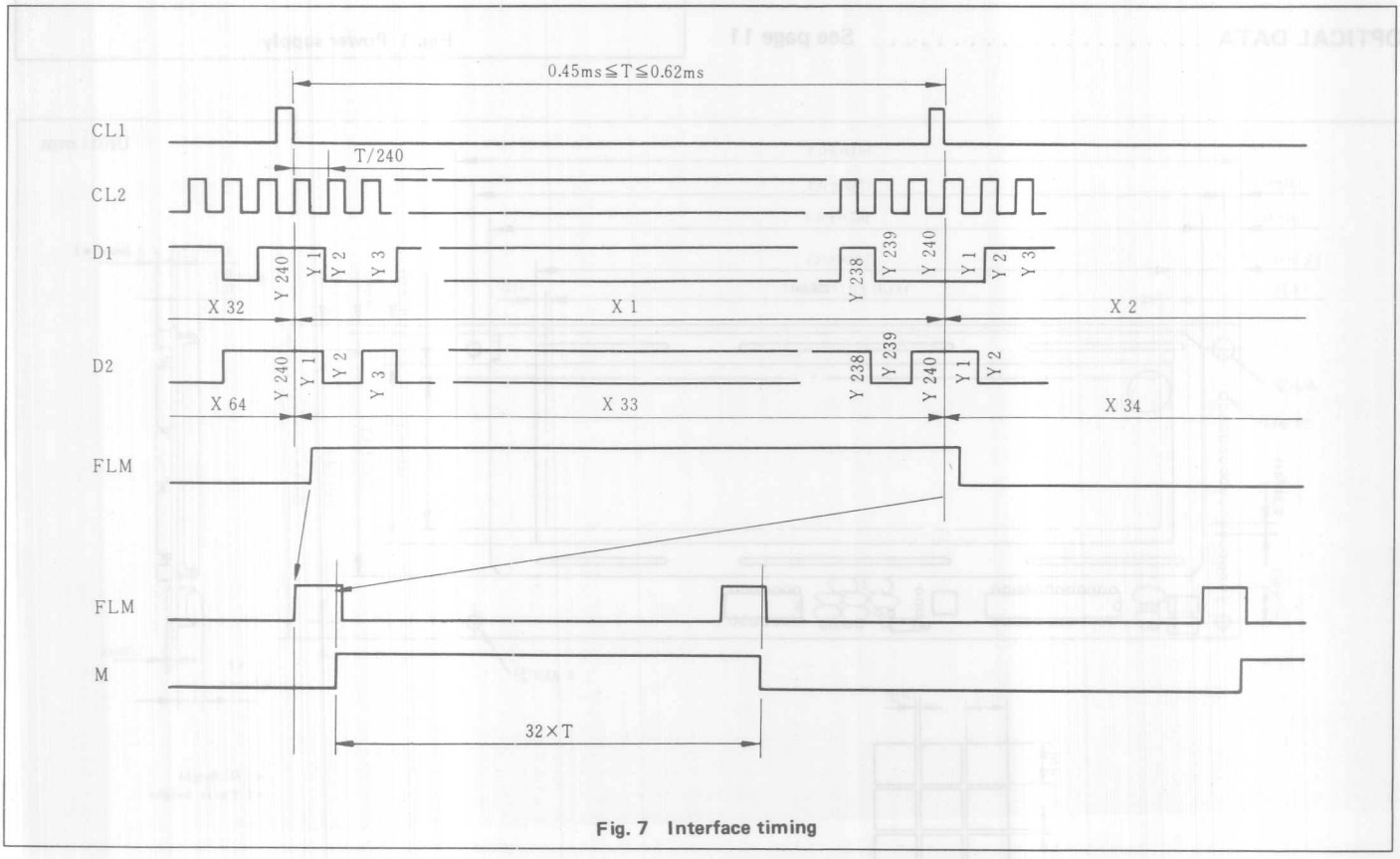


Fig. 7 Interface timing

LM213B

- 256 dot(W) x 64 dot(H) graphic and alpha-numeric display
- Controller LSI HD61830 is built-in (see page 20).

MECHANICAL DATA (Nominal dimensions)

Module size	184W x 75H x 12T (max.) mm
Effective display area	149.6W x 43H mm
Number of dots	256W x 64H mm
Dot size	0.51W x 0.51H mm
Dot pitch	0.56W x 0.56H mm
Weight	about 150 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	15.0 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

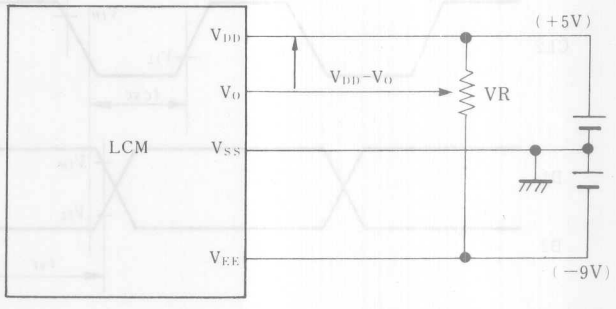
Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V,
V_{EE} = −9.0V $^{+5\%}_{-10\%}$

Operating internal frequency F_{CP1}	500 kHz
F_{CP2}	1.2 MHz
Power consumption	250 mW
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$) Duty = 1/64	
Ta = 0°C	13.2 V typ.
Ta = 25°C	11.7 V typ.
Ta = 40°C	10.2 V typ.

OPTICAL DATA ..... See page 11

INTERFACE TABLE

Pin No.	Symbol	Pin No.	Symbol
1	V_{SS} (GND)	11	DB4
2	V_{DD} (+5V)	12	DB5
3	V_O	13	DB6
4	RS	14	DB7
5	R/W	15	$\overline{CS}$
6	E	16	$\overline{RES}$
7	DB0	17	V_{EE} (−9 V)
8	DB1	18	N.C
9	DB2	19	N.C
10	DB3	20	N.C



V_{DD}-V_O: LCD driving voltage
VR: 10 kΩ ~ 20 kΩ

Fig. 1 Power supply

Unit: mm

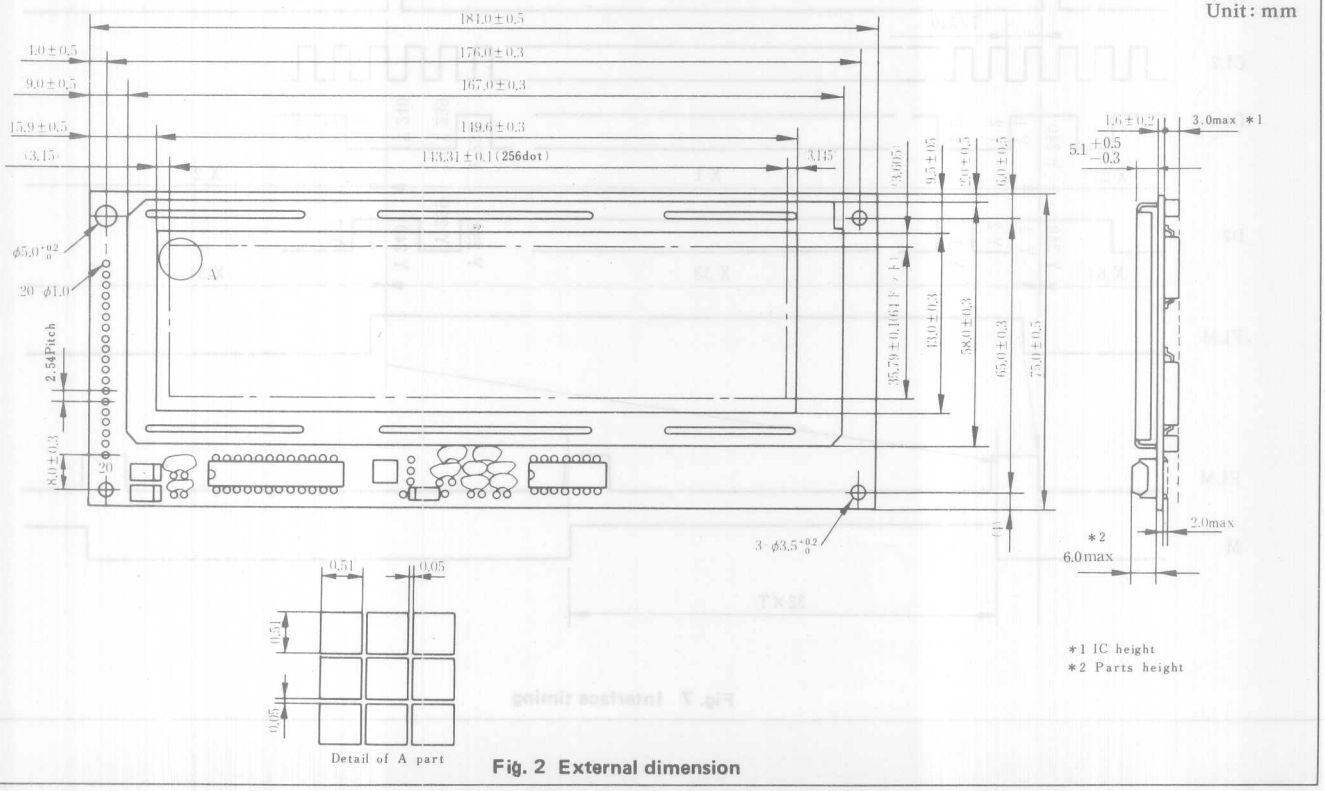


Fig. 2 External dimension

HITACHI

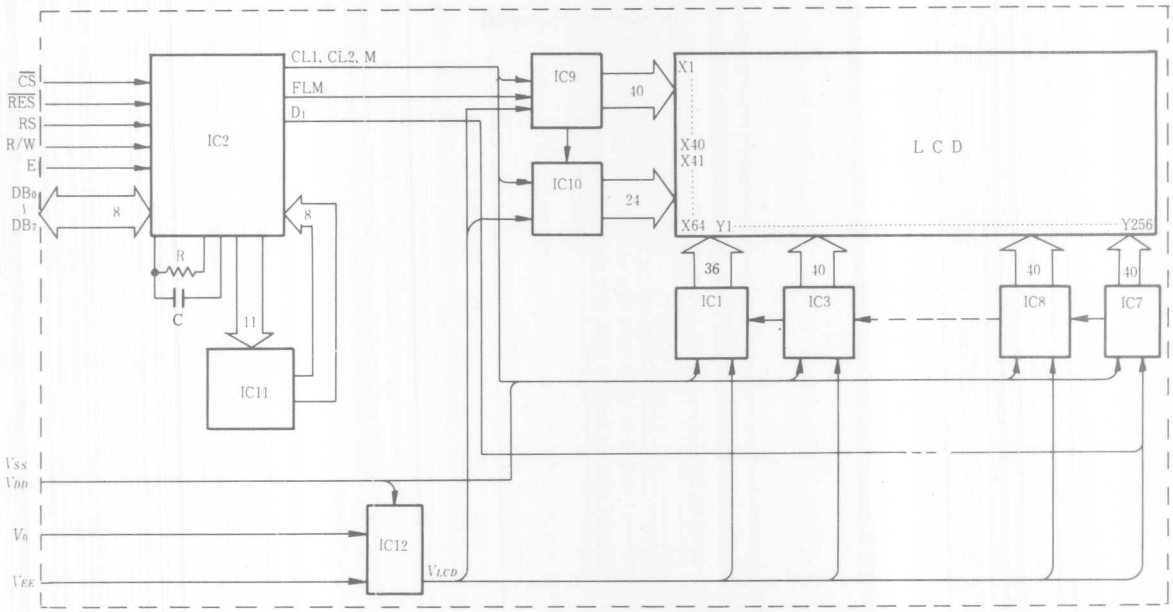


Fig. 3 Block diagram

TIMING CHARACTERISTICS

Item		Symbol	Min.	Typ.	Max.	Unit
Cycle time of 'E'		t_{CYC}	1.0	–	–	μs
Pulse width of 'E'	H level	t_{WEH}	0.45	–	–	μs
	L level	t_{WEL}	0.45	–	–	μs
Pulse raise time of 'E'		t_{Er}	–	–	25	ns
Pulse fall time of 'E'		t_{Ef}	–	–	25	ns
Set up time of CS, R/W, RS		t_{AS}	140	–	–	ns
Set up time of Input Data		t_{DIS}	225	–	–	ns
Data delay time		t_{DD}	–	–	225	ns
Hold time of Data		t_H	10	–	–	ns
Hold time of CS, R/W, RS		t_{AS}	10	–	–	ns

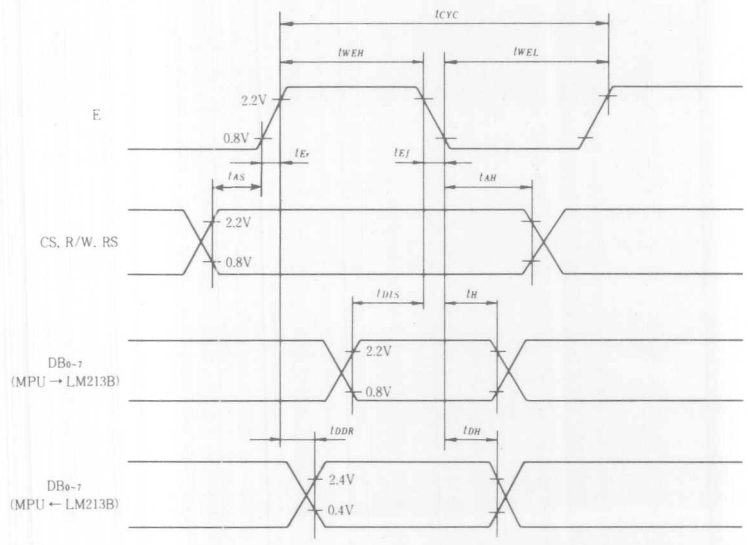


Fig. 4 Interface timing (MPU ⇔ LM213B)

LM211B

- 480 dot(W) x 64 dot(H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see page 20).

MECHANICAL DATA (Nominal dimensions)

Module size	270W x 82H x 13T (max.) mm
Effective display area	240W x 38H mm
Number of dots	480W x 64H dot
Dot size	0.44W x 0.44H mm
Dot pitch	0.49W x 0.49H mm
Weight	about 180 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	15 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	–20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V,
V_{EE} = –9.0V ± 0.45 V

Input "high" voltage (Vi_H)	0.7 x V_{DD} V min.
Input "low" voltage (Vi_L)	0.3 x V_{DD} V max.
Clock frequency (f_{CL2})	610 kHz min.
	920 kHz typ.
	1200 kHz max.
Power supply current (I_{DD})	16 mA typ.
(I_{EE})	6 mA typ.

Power supply for LCD drive (Recommended) ($V_{DD} - V_O$)
Duty = 1/64

Ta = 0°C	13.3 V typ.
Ta = 25°C	11.9 V typ.
Ta = 40°C	10.6 V typ.

OPTICAL DATA . . . . . See page 11

INTERFACE TABLE

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data (left half)
2	FLM	H	The FLM signal indicates the beginning of each display cycle
3	M	H/L	Control signal for AC driving
4	CL1	H→L	The CL1 latches the serial data in the shift registers
5	CL2	H→L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data (right half)
7	V_{DD}(+5V)	–	Power supply for logic circuit
8	V_{SS}	–	Ground
9	V_{EE}(–9V)	–	Power supply for LC driving
10	V_O	–	Operating voltage for LC driving

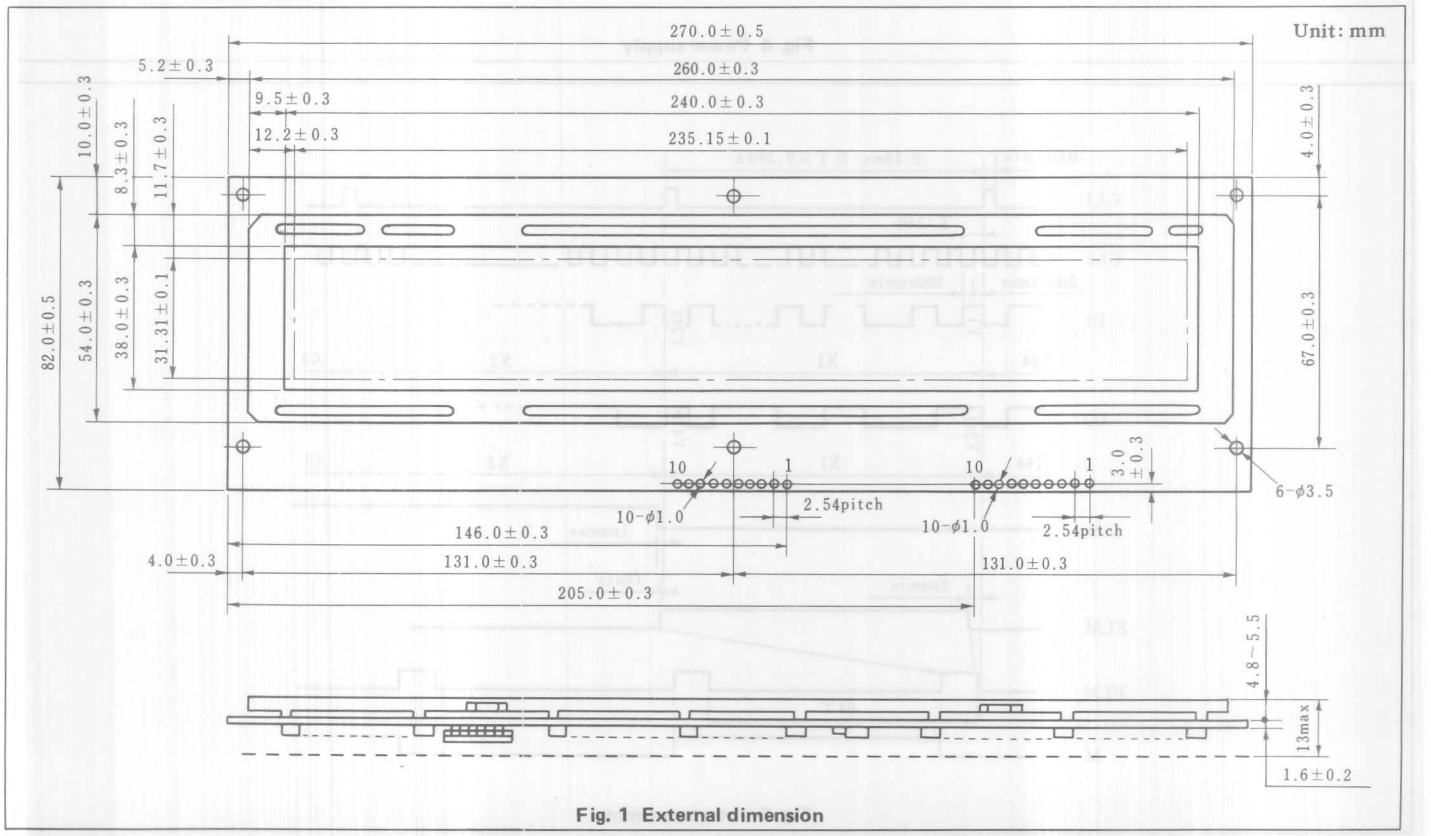


Fig. 1 External dimension

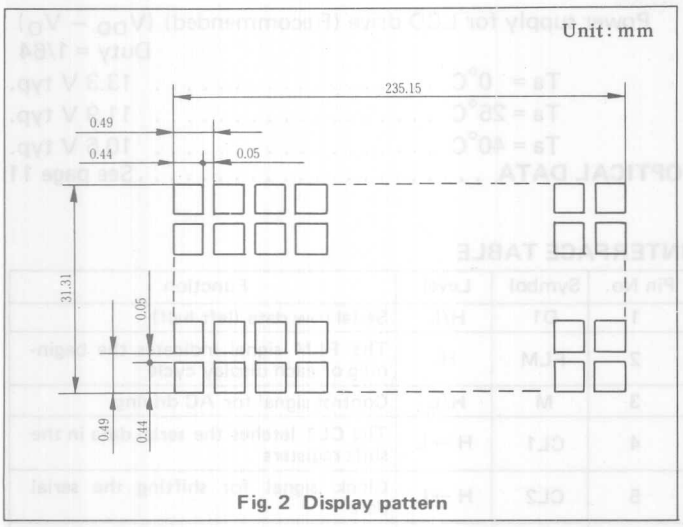


Fig. 2 Display pattern

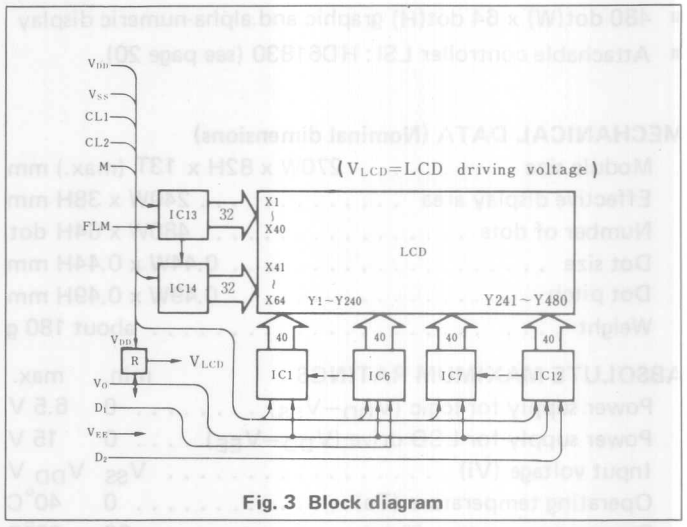
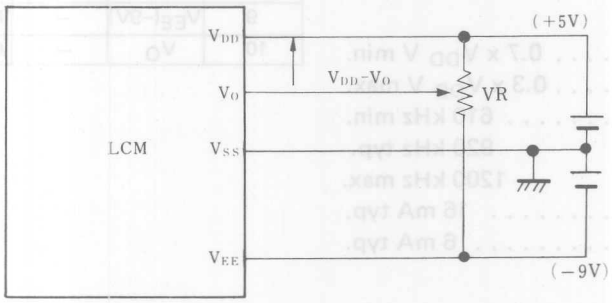


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10 kΩ ~ 20 kΩ

Fig. 4 Power supply

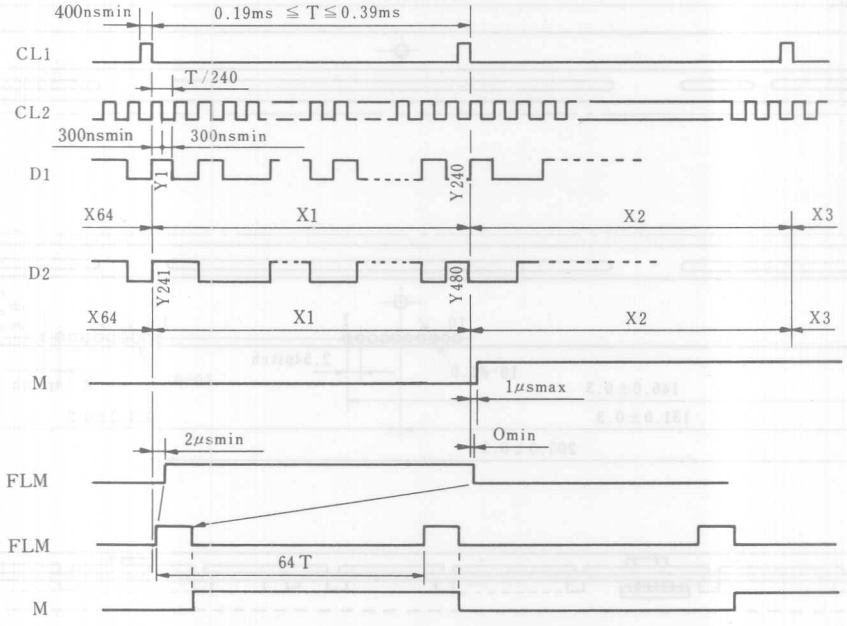


Fig. 5 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CL2}	–	–	1200	kHz (Note 1)
Clock pulse width (High level)	t_{CWH1}	400	–	–	ns
	t_{CWH}	300	–	–	
Clock pulse width (Low level)	t_{CWL}	300	–	–	ns
Clock set up time	t_{CSU}	300	–	–	ns
Data set up time	t_{SU}	200	–	–	ns
FLM set up time	t_{FSU}	200	–	–	ns
M delay time	t_{DM}	−1000	–	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	200	–	–	ns

Notes 1. Optimum frequency for the highest contrast depends on the type of module.
2. Timing of M signal to CL1 may be in the range of ±1000ns.
3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ±2 Hz or 60 Hz ±2 Hz) to prevent LCD flicker.

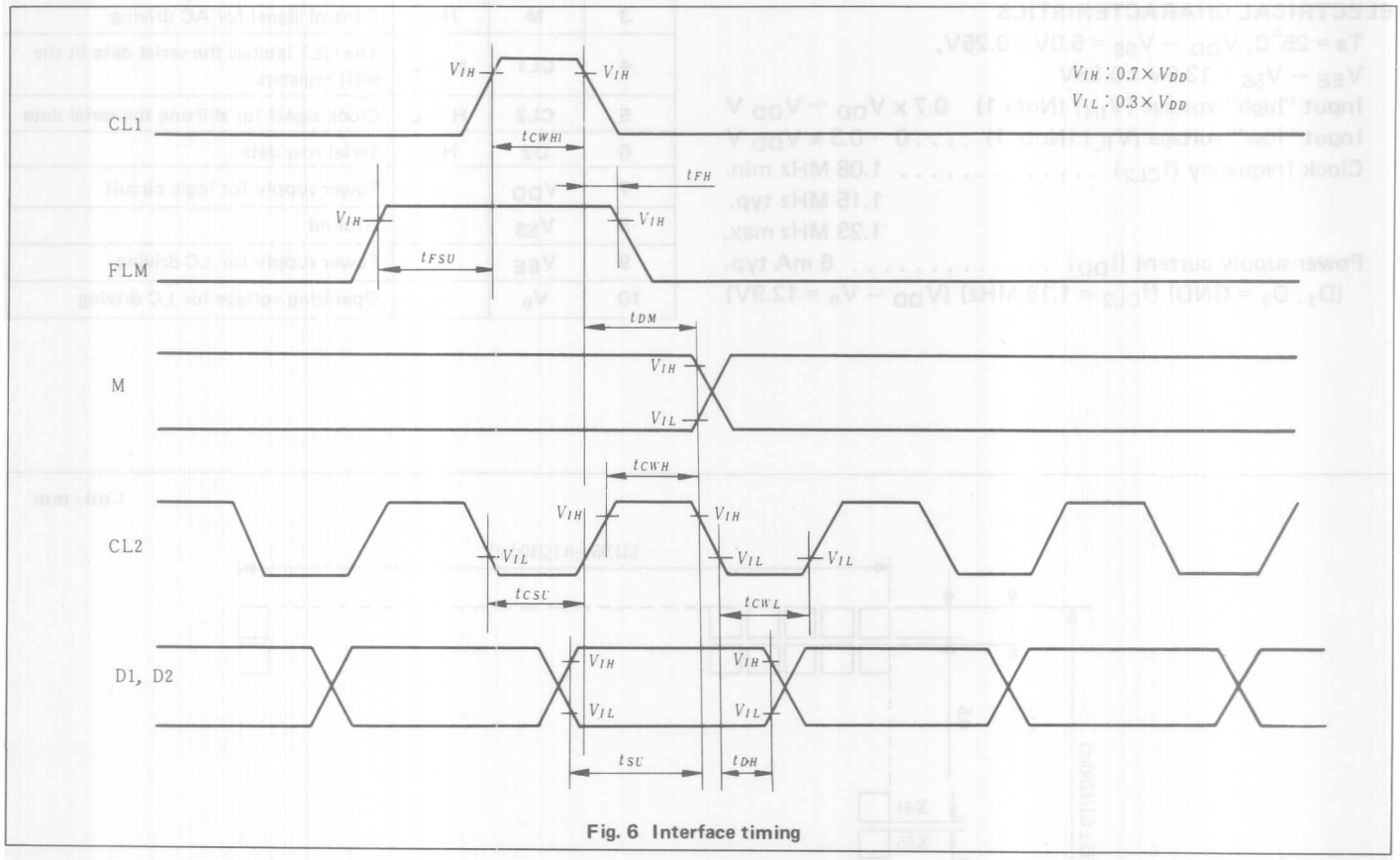


Fig. 6 Interface timing

LM221B

- 240 dot (W) x 128 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see page 20).

MECHANICAL DATA (Nominal dimensions)

Module size	180W x 120H x 13.8T (max.) mm
Effective display area	148W x 75.0H mm
Number of dots	240W x 128H dot
Dot size	0.50W x 0.50H mm
Dot pitch	0.55W x 0.55H mm
Weight	about 210 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	19.0 V
Input voltage (Vi) (Note 1)	V_{SS}	V_{DD} V
Operating temperature (Ta) (Note 2)	0	50°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, $V_{DD} - V_{SS}$ = 5.0V ±0.25V,
$V_{EE} - V_{SS}$ = 13.5V ±0.25V

Input "high" voltage (V_{IH}) (Note 1)	0.7 x V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL}) (Note 1)	0 ~ 0.3 x V_{DD} V
Clock frequency (f_{CL2})	1.08 MHz min.
	1.15 MHz typ.
	1.23 MHz max.
Power supply current (I_{DD})	6 mA typ.

(D_1, D_2 = GND) (f_{CL2} = 1.15 MHz) ($V_{DD} - V_0$ = 12.9V)

Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/64

Ta = 0°C	14.9 V typ.
Ta = 25°C	13.7 V typ.
Ta = 40°C	12.3 V typ.

OPTICAL DATA ..... See page 11

Notes 1. Applied to CL1, CL2, D1 ~ D2, M, FLM.
2. When operated at maximum temperature, the display may be changed into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data
2	FLM	H	The FLM signal indicates the beginning of each display cycle
3	M	H/L	Control signal for AC driving
4	CL1	H → L	The CL1 latches the serial data in the shift registers
5	CL2	H → L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data
7	V_{DD}	—	Power supply for logic circuit
8	V_{SS}	—	Ground
9	V_{EE}	—	Power supply for LC driving
10	V_0	—	Operating voltage for LC driving

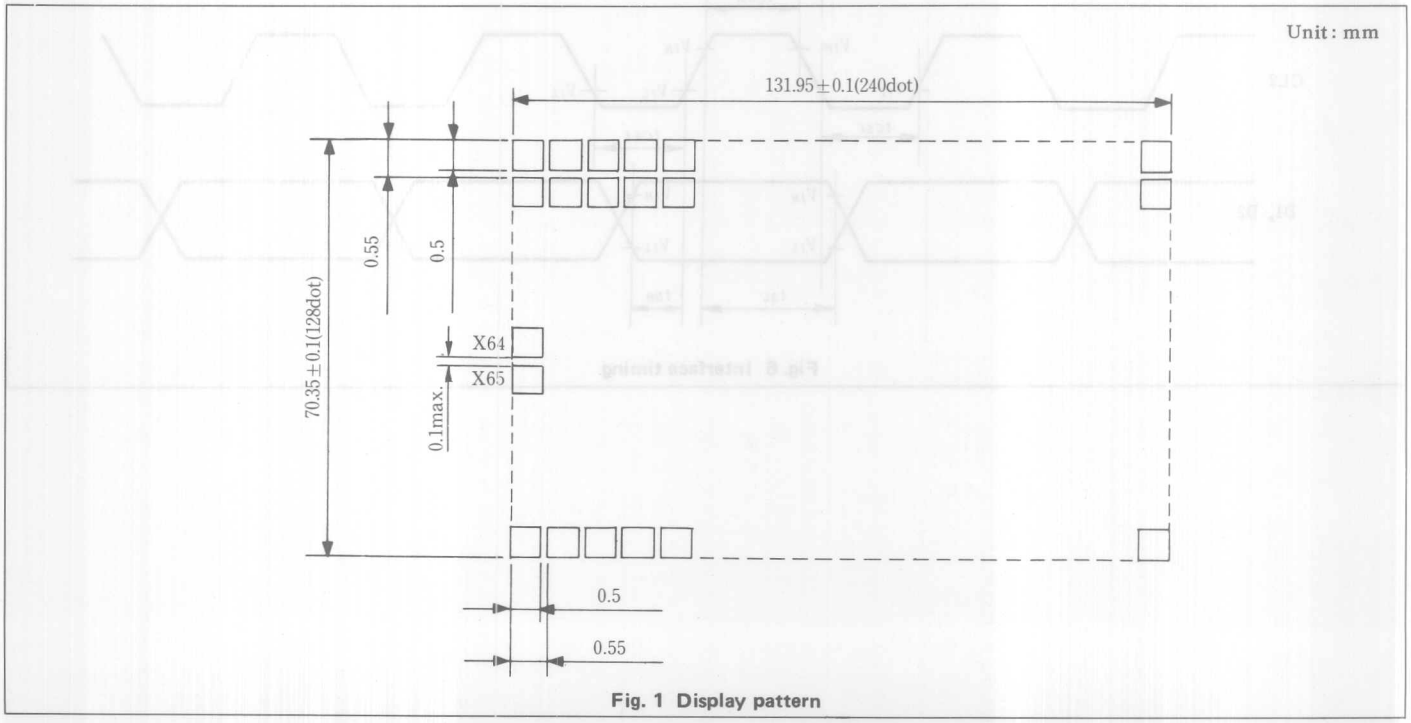


Fig. 1 Display pattern

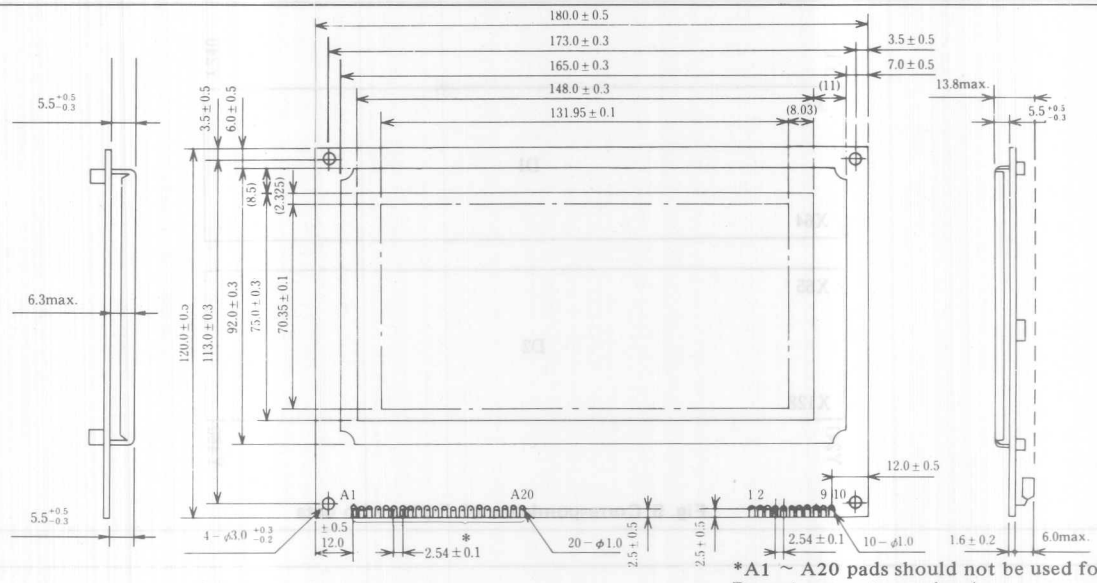


Fig. 2 External dimensions

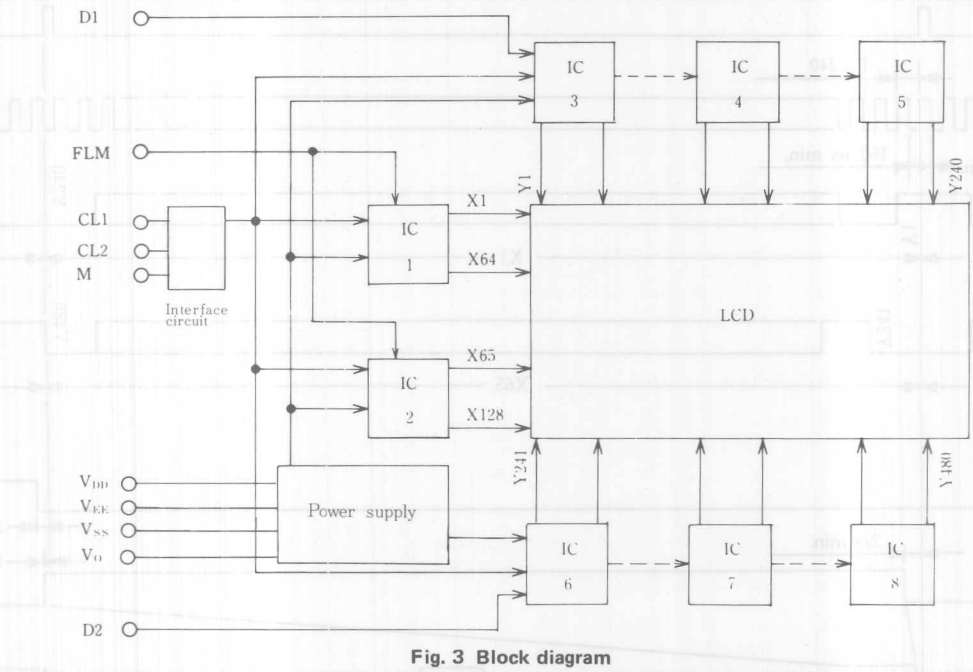
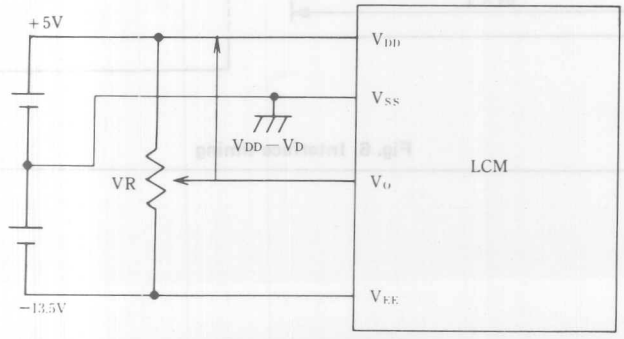


Fig. 3 Block diagram



VDD − VO: LCD driving voltage
VR: 10kΩ ~ 20kΩ

Fig. 4 Power supply

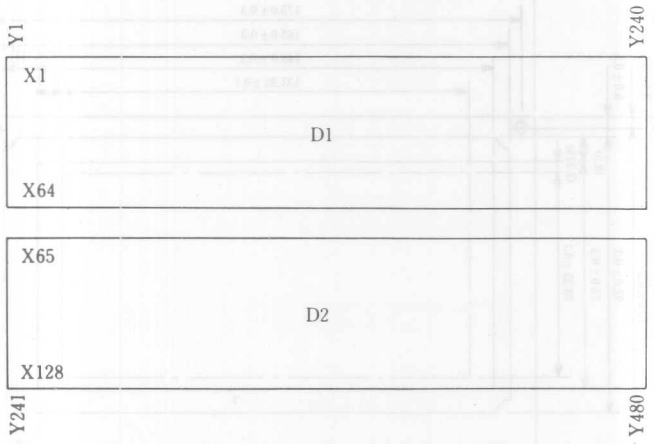


Fig. 5 Correspondence of display with data

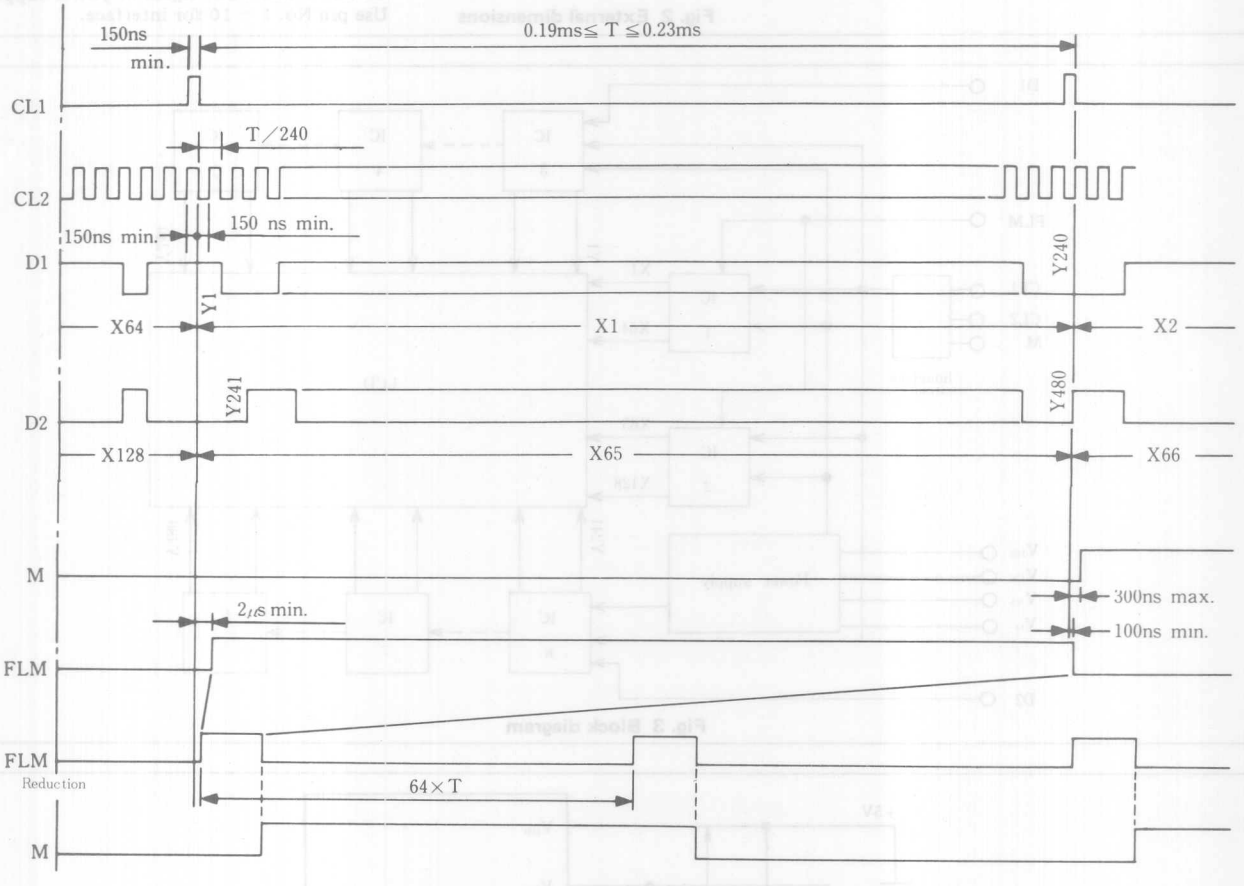


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	810	–	–	ns
CL2 pulse width (H)	t_{CWH}	150	–	–	ns
CL2 pulse width (L)	t_{CWL}	150	–	–	ns
CL1 set up time (1)	t_{SCL1}	150	–	–	ns
CL1 set up time (2)	t_{HCL1}	150	–	–	ns
Clock rise/fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
CL1 delay time	t_{CL}	150	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	100	–	–	ns
FLM hold time	t_{FH}	100	–	–	ns

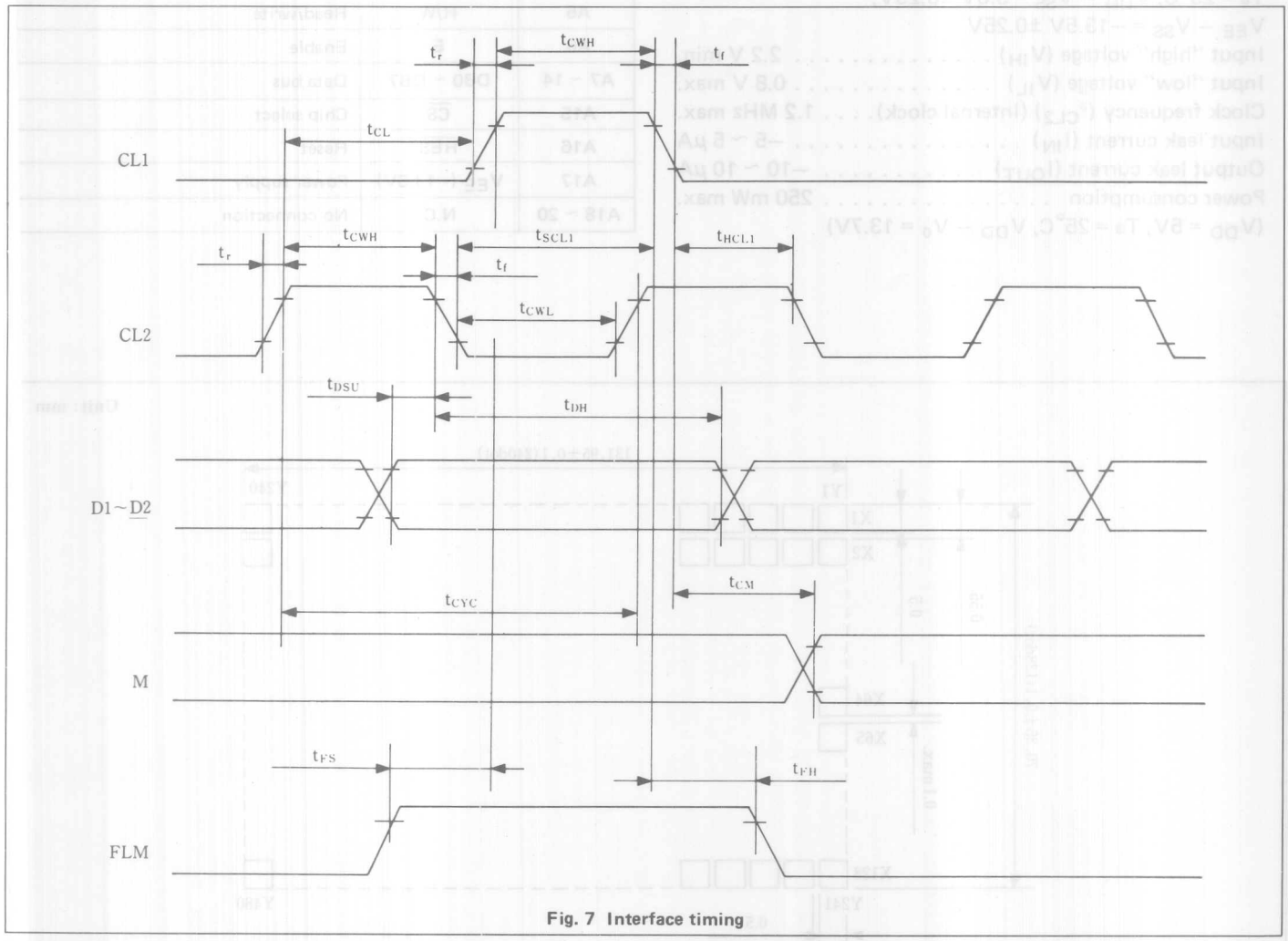


Fig. 7 Interface timing

LM238B

- 240 dot (W) x 128 dot (H) graphic and alpha-numeric display
- Controller LSI HD61830 is built-in. (see page 20).

MECHANICAL DATA (Nominal dimensions)

Module size	180W x 120H x 13.8T (max.) mm
Effective display area	148W x 75.0H mm
Number of dots	240W x 128H dot
Dot size	0.50W x 0.50H mm
Dot pitch	0.55W x 0.55H mm
Weight	about 220 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	19.0 V
Input voltage (Vi) (Note 1)	V_{SS}	V_{DD} V
Operating temperature (Ta) (Note 2)	0	50°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, $V_{DD} - V_{SS}$ = 5.0V ±0.25V,
$V_{EE} - V_{SS}$ = −13.5V ±0.25V

Input "high" voltage (V_{IH})	2.2 V min.
Input "low" voltage (V_{IL})	0.8 V max.
Clock frequency (f_{CL2}) (Internal clock)	1.2 MHz max.
Input leak current (I_{IN})	−5 ~ 5 μA
Output leak current (I_{OUT})	−10 ~ 10 μA
Power consumption (V_{DD} = 5V, Ta = 25°C, $V_{DD} - V_0$ = 13.7V)	250 mW max.

Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/64

Ta = 0°C	14.9 V typ.
Ta = 25°C	13.7 V typ.
Ta = 40°C	12.3 V typ.

OPTICAL DATA ..... See page 11

Notes 1. Applied to CL1, CL2, D1 ~ D2, M, FLM.
2. When operated at maximum temperature, the display may be changed into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Function
A1	V_{SS} (0V)	Ground
A2	V_{DD} (+5V)	Power supply for logic
A3	V_0	Power supply for LCD drive
A4	RS	Register select
A5	R/W	Read/write
A6	E	Enable
A7 ~ 14	DB0 ~ DB7	Data bus
A15	$\overline{CS}$	Chip select
A16	$\overline{RES}$	Reset
A17	V_{EE} (−13.5V)	Power supply
A18 ~ 20	N.C	No connection

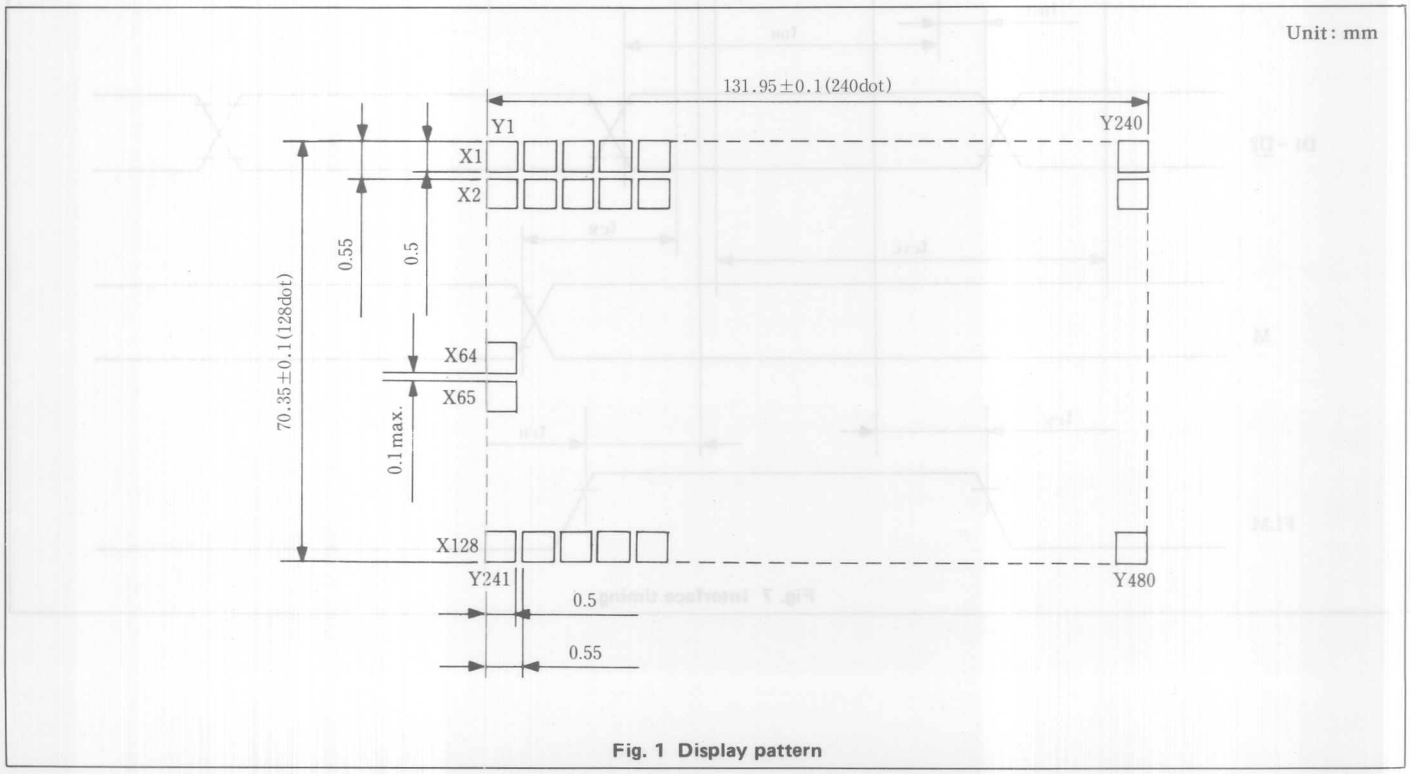
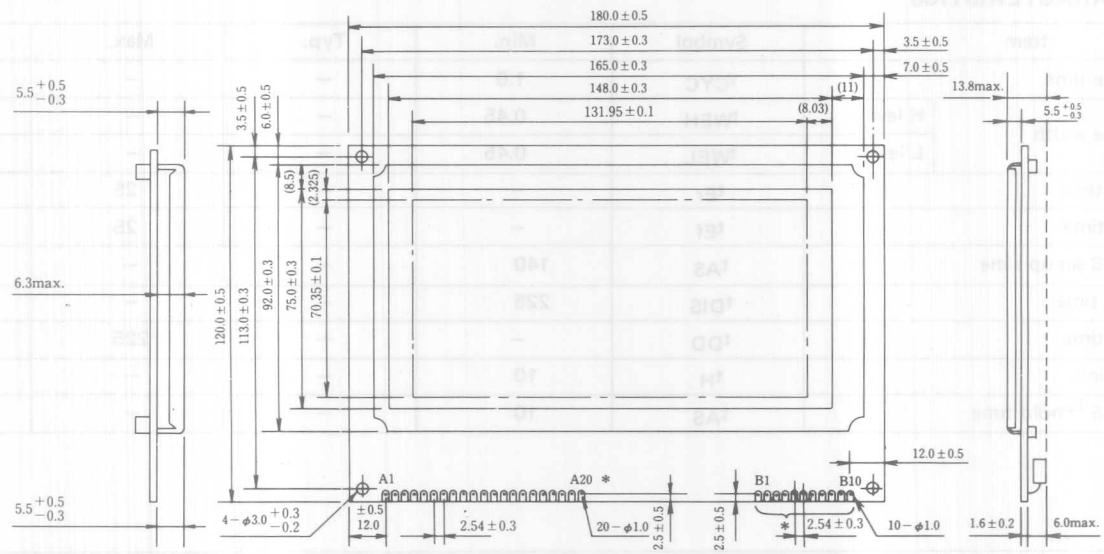


Fig. 1 Display pattern

HITACHI

Unit: mm



*B1 ~ B10 pads should not be used for LM238B.
Do not connect any signal or power supply.
Use A1 ~ A20 for interface.

Fig. 2 External dimension

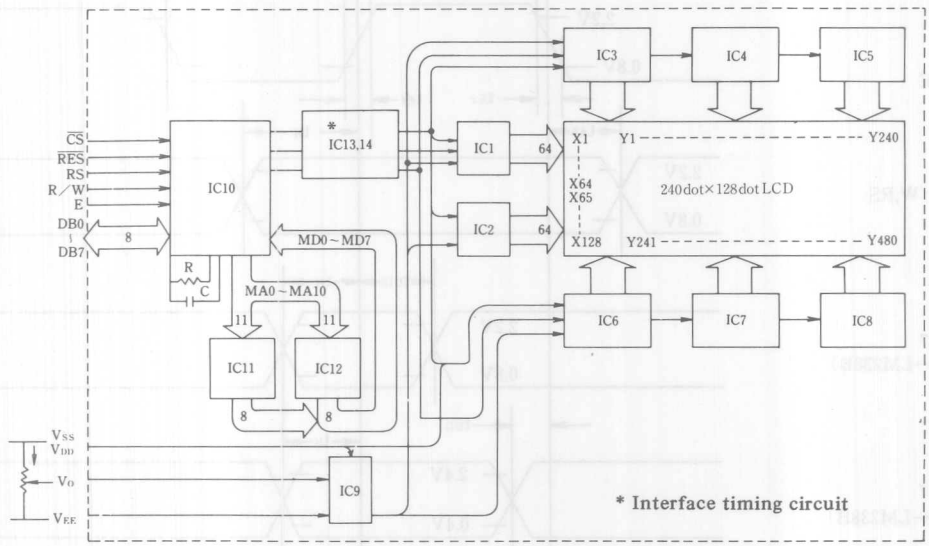


Fig. 3 Block diagram

$V_{DD} - V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

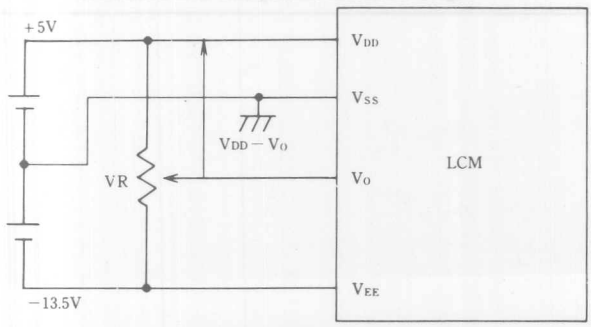


Fig. 4 Power supply

$V_{DD} - V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

TIMING CHARACTERISTICS

Item		Symbol	Min.	Typ.	Max.	Unit
Enable cycle time		t_{CYC}	1.0	–	–	μs
Enable pulse width	H level	t_{WEH}	0.45	–	–	μs
	L level	t_{WEL}	0.45	–	–	μs
Enable rise time		t_{Er}	–	–	25	ns
Enable fall time		t_{Ef}	–	–	25	ns
CS, R/W, RS set up time		t_{AS}	140	–	–	ns
Data set up time		t_{DIS}	225	–	–	ns
Data delay time		t_{DD}	–	–	225	ns
Data hold time		t_H	10	–	–	ns
CS, R/W, RS →hold time		t_{AS}	10	–	–	ns

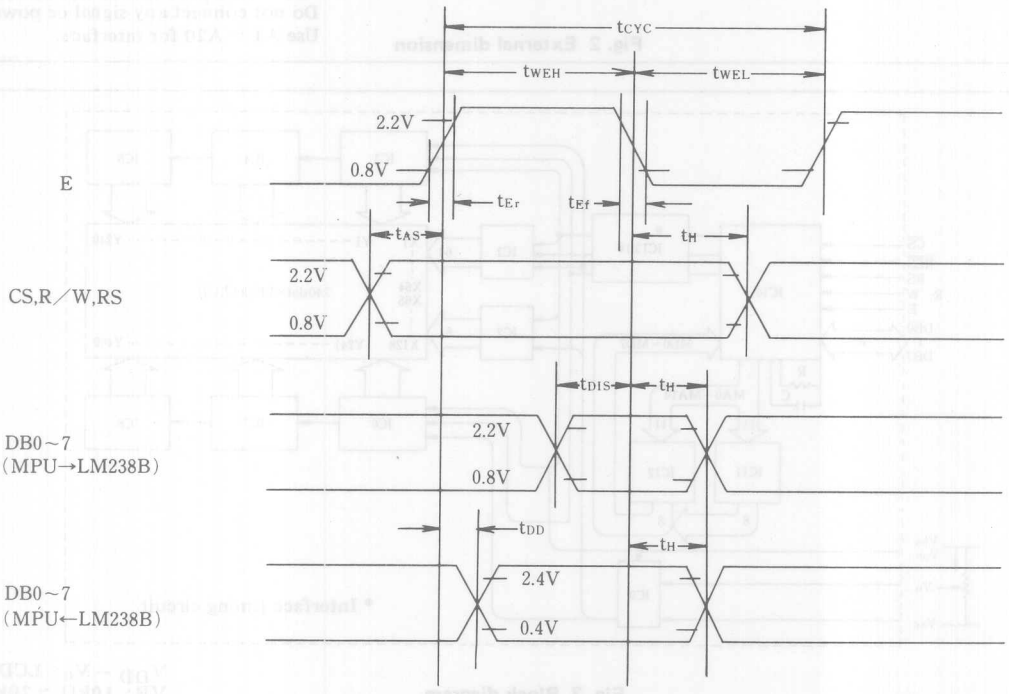


Fig. 5 Interface timing (MPU ↔ LM238B)

LM215B·LM215SB

- 480 dot (W) x 128 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see page 20).

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 270W x 110H x 11.5T (max.) mm
Effective display area . . . . . 242W x 69H mm
Number of dots . . . . . 480W x 128H dot
Dot size . . . . . 0.43W x 0.43H mm
Dot pitch . . . . . 0.48W x 0.48H mm
Weight . . . . . about 320 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	19.0 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD} V
Operating temperature (Ta) (Note 2)	0	50°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V,
V_{EE} = −10.0 V ±0.25 V
Input "high" voltage (V_{IH}) (Note 1) . 0.7 x V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL}) (Note 1) . . . . 0 ~ 0.3 x V_{DD} V
Clock frequency (f_{CL2}) . . . . . 1.08 MHz min.
1.15 MHz typ.
1.23 MHz max.
Power supply current (I_{DD}) . . . . . 6 mA typ.
(I_{EE}) . . . . . 3 mA typ.
(D_1 ~ D_4 = GND) (f_{CL2} = 1.15 MHz) ($V_{DD} - V_0$ = 11.9V) (LM215B)·12.5V (LM215SB)
Power supply for LCD drive (Recommended)($V_{DD} - V_0$)
Duty = 1/64

	LM215B	LM215SB
Ta = 0°C	13.3	13.6 V typ.
Ta = 25°C	11.9	12.5 V typ.
Ta = 40°C	10.6	11.9 V typ.

OPTICAL DATA . . . . . See page 11

Notes 1. Applied to D1 ~ D4, FLM, M, CL1, CL2.
2. When operated at maximum temperature, the display may be changed into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data (upper left half)
2	D2	H/L	Serial row data (lower left half)
3	FLM	H	The FLM signal indicates the beginning of each display cycle
4	M	H/L	Control signal for AC driving
5	CL1	H→L	The CL1 latches the serial data in the shift registers
6	CL2	H→L	Clock signal for shifting the serial data
7	D3	H/L	Serial row data (upper right half)
8	D4	H/L	Serial row data (lower right half)
9	V_{DD}(+5V)	—	Power supply for logic circuit
10	V_{SS} (0V)	—	Ground
11	VEE(−10V)	—	Power supply for LC driving
12	V_O	—	Operating voltage for LC driving

Unit: mm

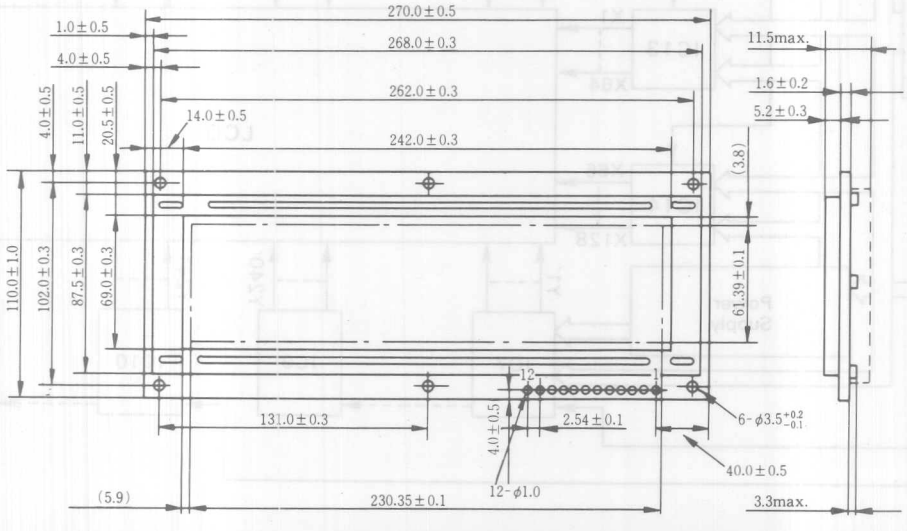


Fig. 2 Display pattern

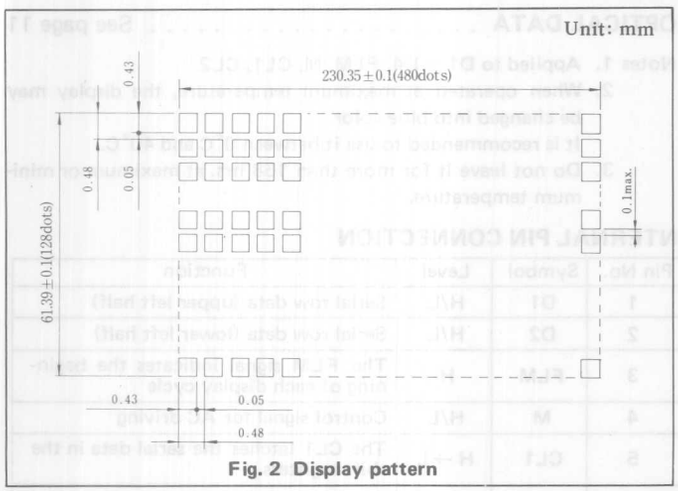


Fig. 2 Display pattern

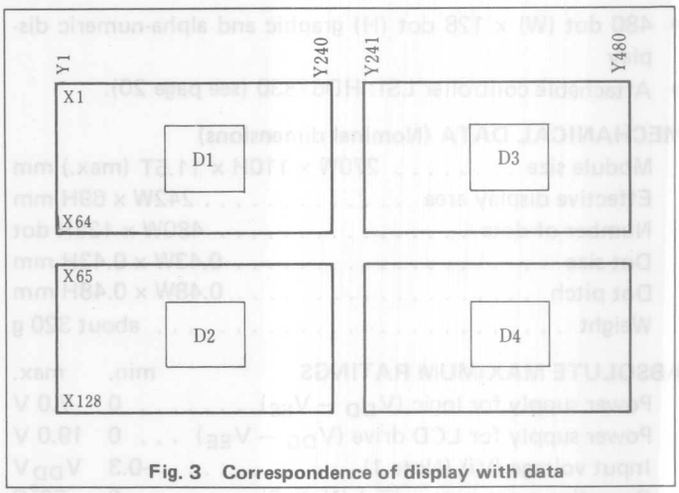
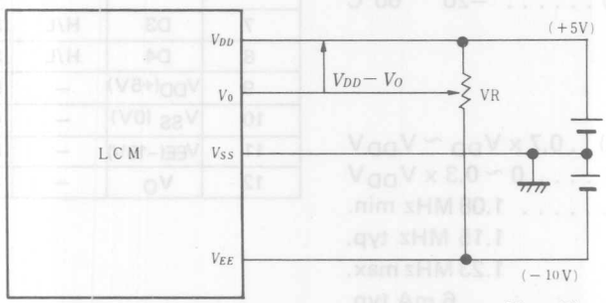
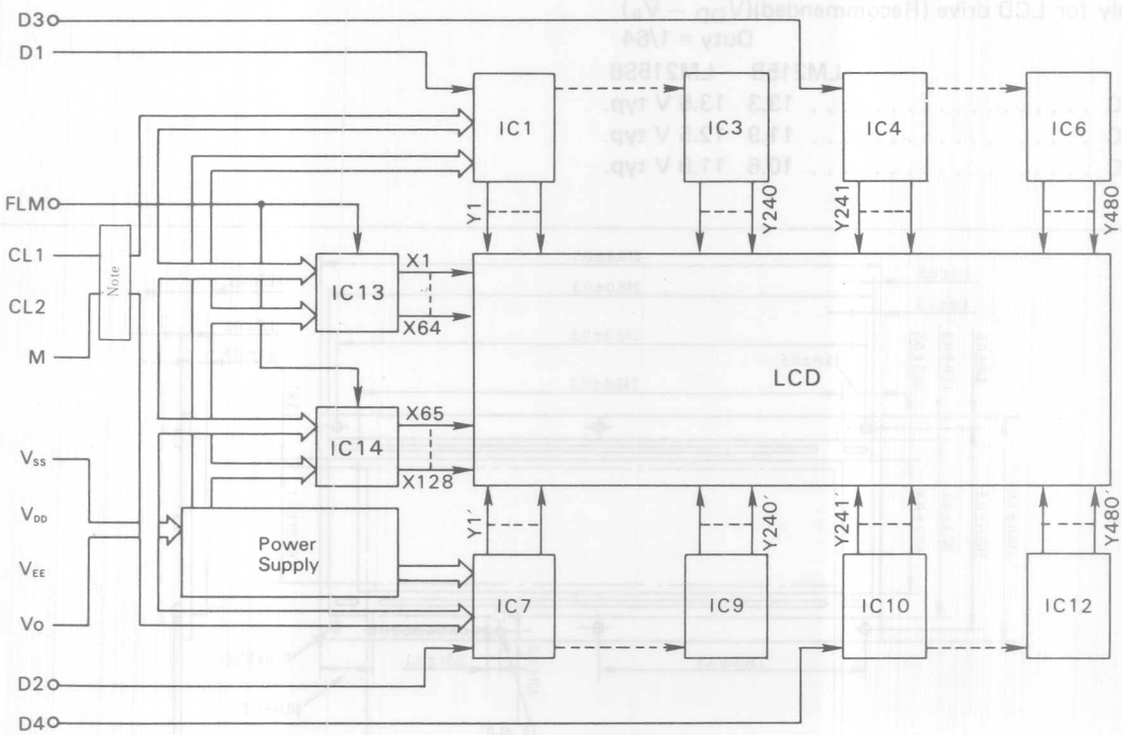


Fig. 3 Correspondence of display with data



V_{DD}-V_O: Operating Voltage for LC driving
VR: 10 kΩ ~ 20 kΩ

Fig. 4 Power supply



Note: Interface timing circuit

Fig. 5 Block diagram

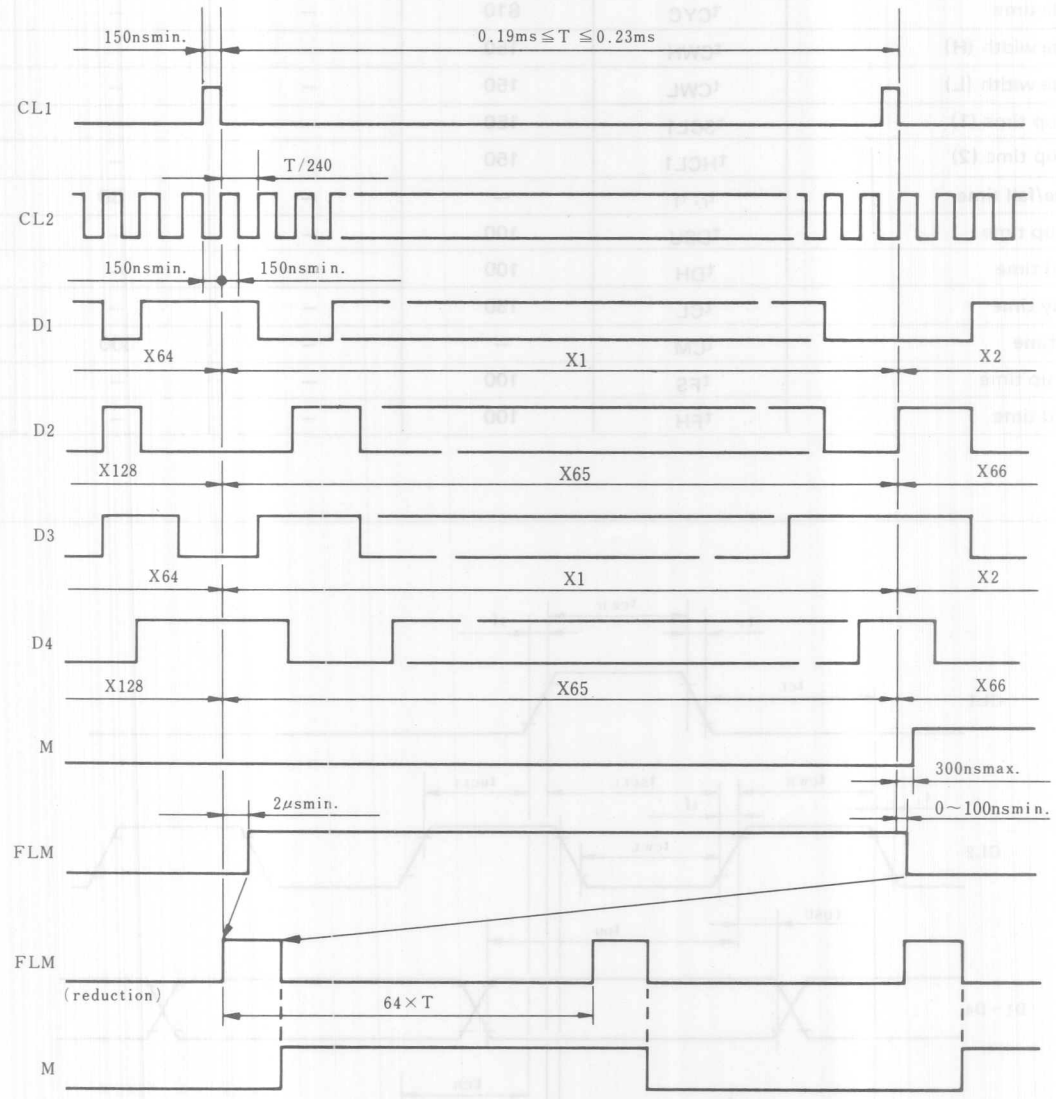


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	810	–	–	ns
CL2 pulse width (H)	t_{CWH}	150	–	–	ns
CL2 pulse width (L)	t_{CWL}	150	–	–	ns
CL1 set up time (1)	t_{SCL1}	150	–	–	ns
CL1 set up time (2)	t_{HCL1}	150	–	–	ns
Clock rise/fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
CL1 delay time	t_{CL}	150	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	100	–	–	ns
FLM hold time	t_{FH}	100	–	–	ns

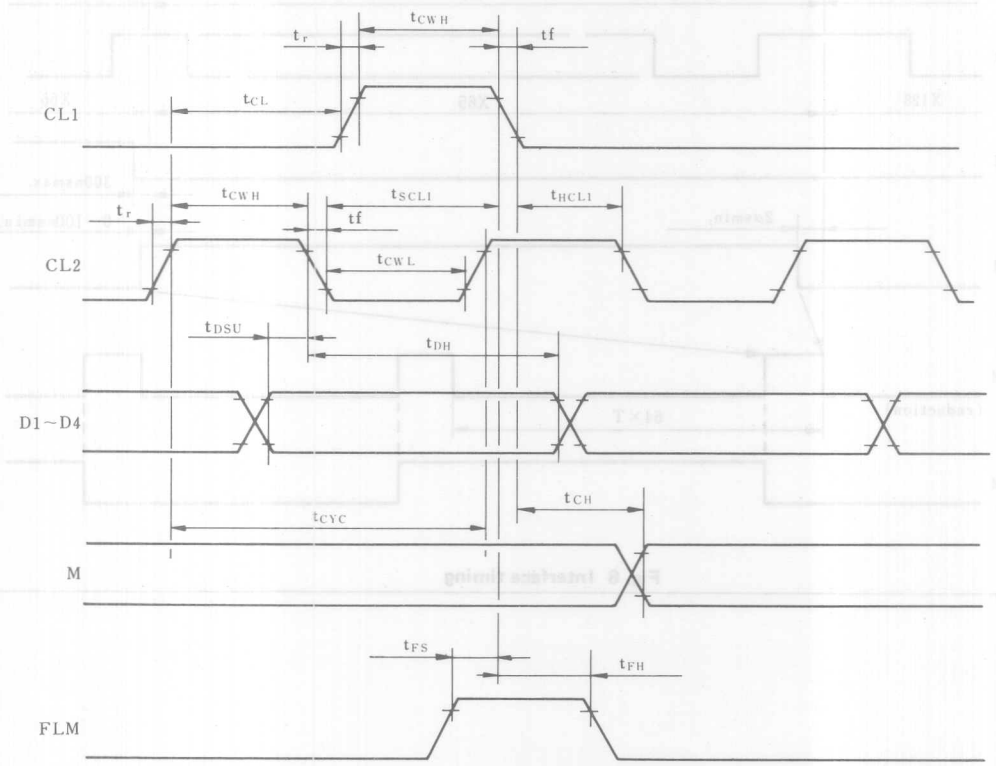


Fig. 7 Interface timing

LM224B

- 480 dot (W) x 128 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830B (see page 20).

MECHANICAL DATA (Nominal dimensions)

Module size	270W x 110H x 11.5T (max.) mm
Effective display area	242W x 69H mm
Number of dots	480W x 128H dot
Dot size	0.43W x 0.43H mm
Dot pitch	0.48W x 0.48H mm
Weight	about 320 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	19.0 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD} V
Operating temperature (Ta) (Note 2)	0	50°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, $V_{DD} - V_{SS}$ = 5.0 V ±0.25 V,
$V_{EE} - V_{SS}$ = 11.0 V ±0.5 V

Input "high" voltage (V_{IH})	0.7 x V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL})	0 ~ 0.3 x V_{DD} V
Clock frequency (f_{CL2})	2.15 MHz min.
	2.30 MHz typ.
	2.40 MHz max.
Power supply current (I_{DD})	10 mA typ.
(I_{EE})	3 mA typ.

(D_1, D_2 = GND) (f_{CL2} = 2.30 MHz) ($V_{DD} - V_0$ = 13.8V)

Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/64

Ta = 0°C	14.8 V typ.
Ta = 25°C	13.8 V typ.
Ta = 40°C	12.4 V typ.

OPTICAL DATA

See page 11

Notes 1. Applied to FLM, M, CL1, CL2, D1, D2.
2. When operated at maximum temperature, the display may be changed into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Data signal
2	D2	H/L	Data signal
3	FLM	H	The FLM signal indicates the beginning of each display cycle
4	M	H/L	Control signal for AC driving
5	CL1	H→L	The CL1 latches the serial data in the shift registers
6	CL2	H→L	Clock signal for shifting the serial data
7	NC	—	Data signal
8	NC	—	Data signal
9	V_{DD}	—	Power supply for logic circuit
10	V_{SS}	—	Ground
11	V_{EE}	—	Power supply for LC driving
12	V_O	—	Operating voltage for LC driving

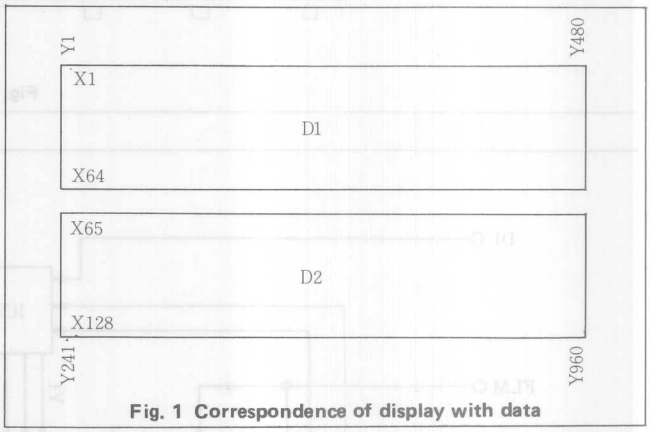


Fig. 1 Correspondence of display with data

Unit: mm

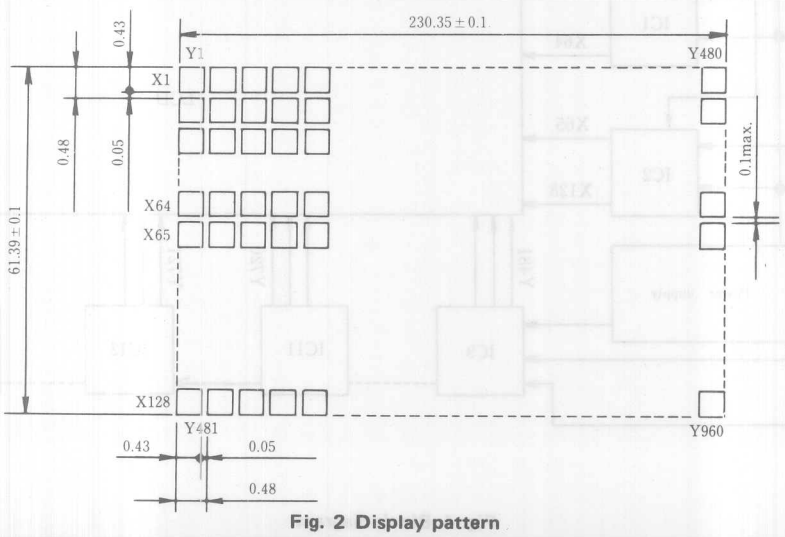


Fig. 2 Display pattern

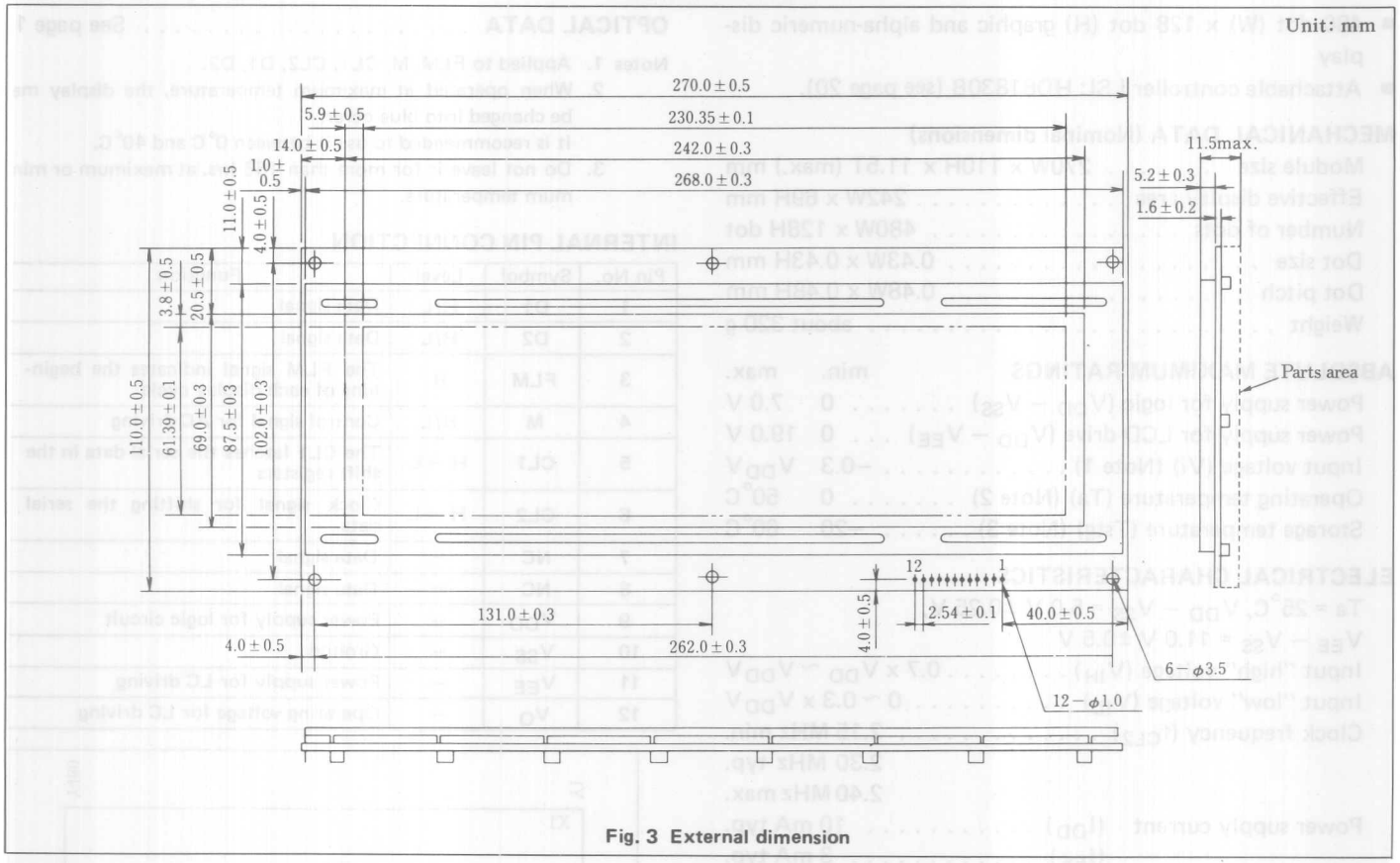


Fig. 3 External dimension

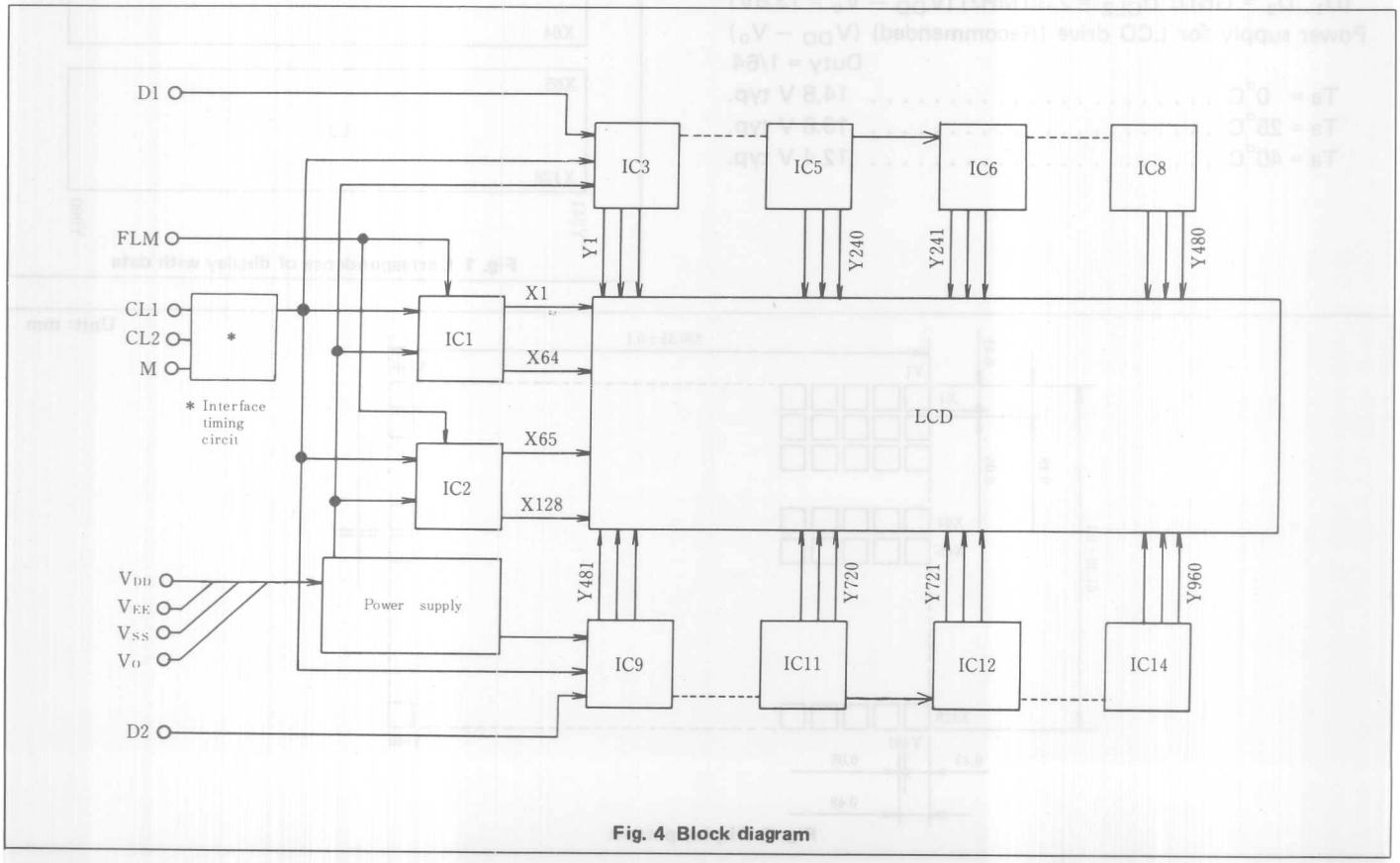


Fig. 4 Block diagram

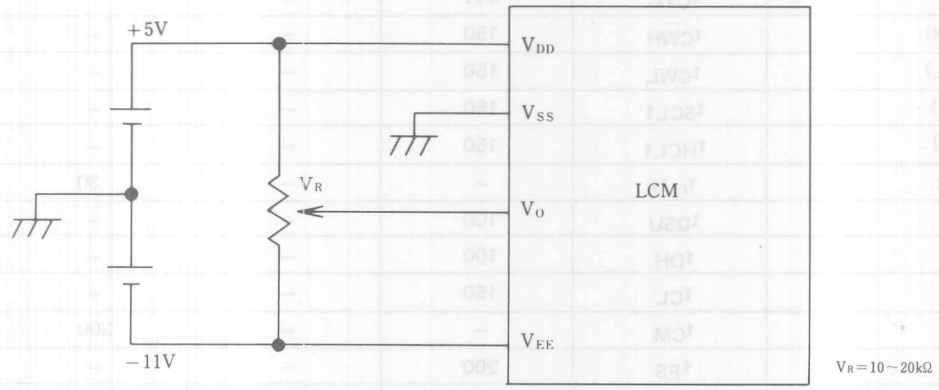


Fig. 5 Power supply

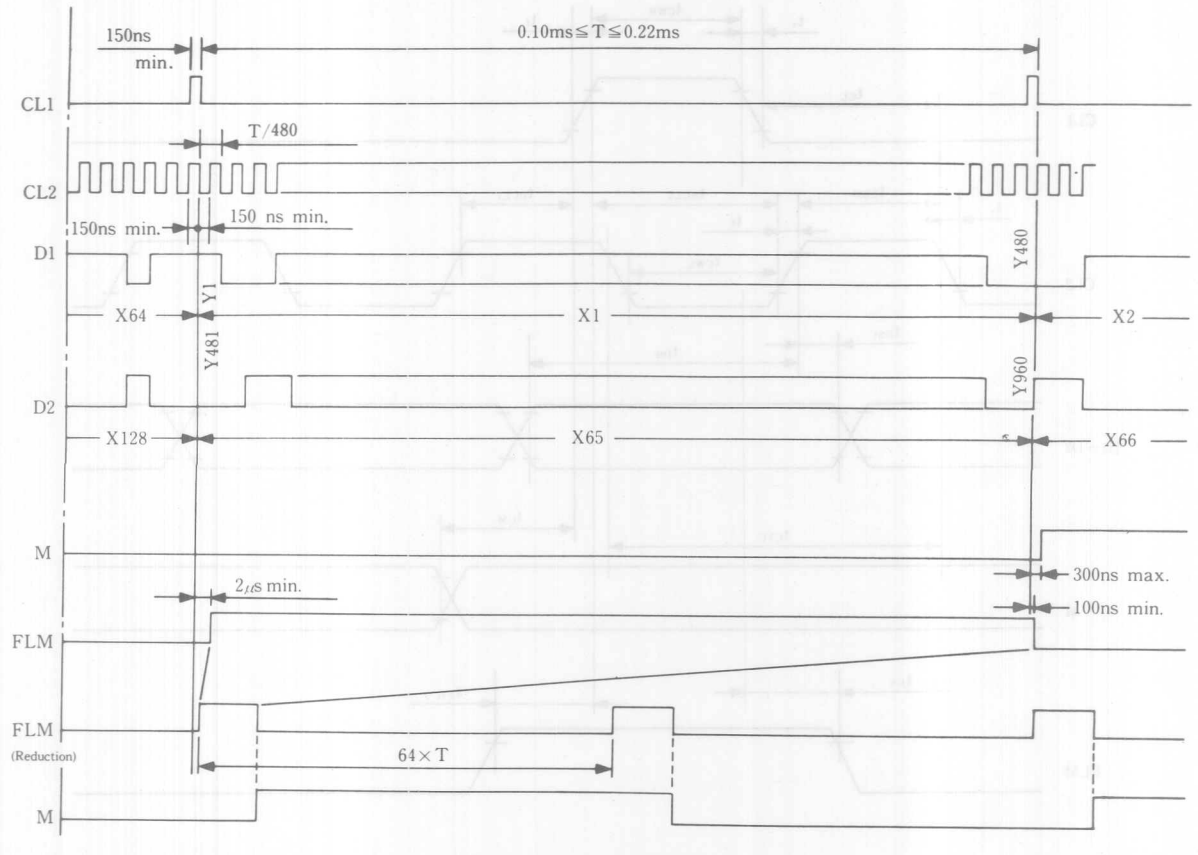


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	417	–	–	ns
CL2 pulse width (H)	t_{CWH}	150	–	–	ns
CL2 pulse width (L)	t_{CWL}	150	–	–	ns
CL1 set up time (1)	t_{SCL1}	150	–	–	ns
CL1 set up time (2)	t_{HCL1}	150	–	–	ns
Clock rise/fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
CL1 delay time	t_{CL}	150	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	200	–	–	ns
FLM hold time	t_{FH}	100	–	–	ns

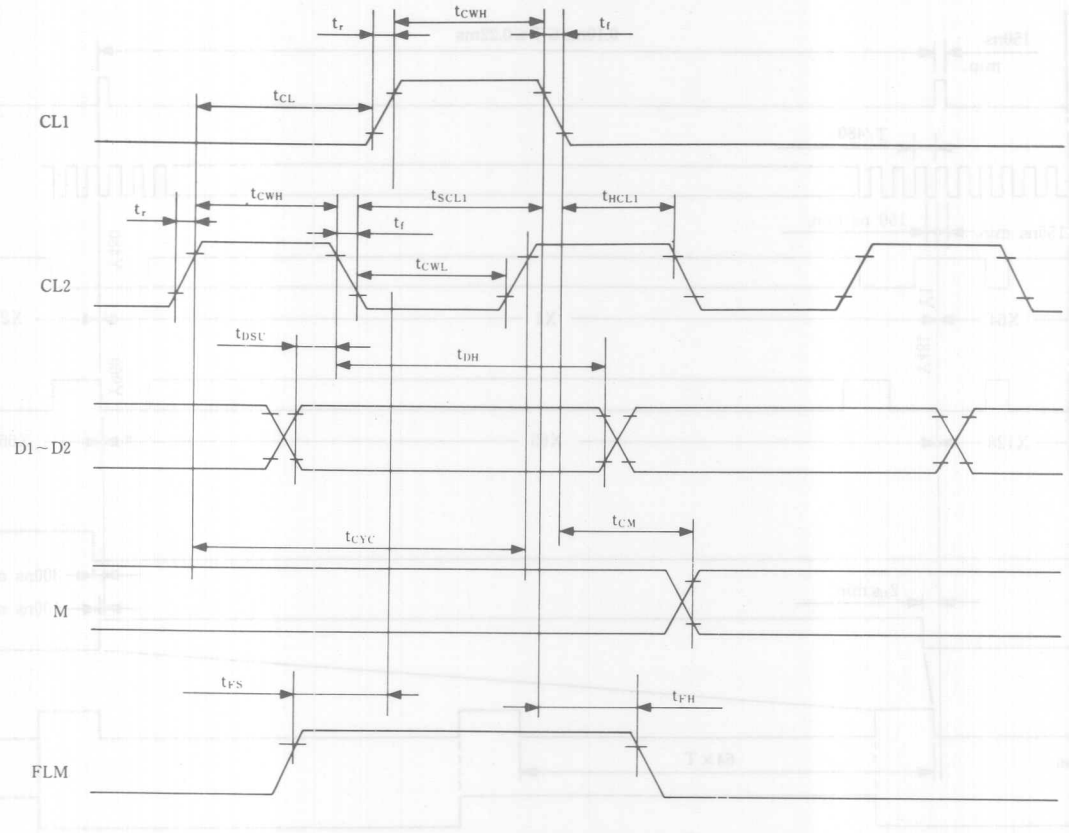


Fig. 7 Interface timing

LM225S

- 640 dot (W) x 200 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see page 20).

MECHANICAL DATA (Nominal dimensions)

Module size	270W x 150H x 13.0T (max.) mm
Effective display area	239W x 104H mm
Number of dots	640W x 200H dot
Dot size	0.32W x 0.46H mm
Dot pitch	0.35W x 0.49H mm
Weight	about 450 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	19.0 V
Input voltage (Vi) (Note 1)	V_{SS}	V_{DD} V
Operating temperature (Ta) (Note 2)	0	50°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, $V_{DD} - V_{SS}$ = 5.0 V ±0.25 V,
$V_{EE} - V_{SS}$ = −13.5 V ±0.25 V

Input "high" voltage (V_{IH})	0.7 x V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL})	0 ~ 0.3 x V_{DD} V
Clock frequency (f_{CL2})	2.13 MHz min.
	2.28 MHz typ.
	2.46 MHz max.
Power supply current (I_{DD})	6 mA typ.
(I_{EE})	3 mA typ.

(D_1, D_2 = GND) (f_{CL2} = 2.28 MHz) ($V_{DD} - V_0$ = 14.0V)
(D_3, D_4 = GND)

Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/100

Ta = 0°C	15.0 V typ.
Ta = 25°C	14.0 V typ.
Ta = 40°C	13.0 V typ.

OPTICAL DATA

See page 11

Notes 1. Applied to CL1, CL2, D1 ~ D4, M, FLM.
2. When operated at maximum temperature, the display may be changed into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data (upper left half)
2	D2	H/L	Serial row data (lower left half)
3	FLM	H	The FLM signal indicates the beginning of each display cycle
4	M	H/L	Control signal for AC driving
5	CL1	H→L	The CL1 latches the serial data in the shift registers
6	CL2	H→L	Clock signal for shifting the serial data
7	D3	H/L	Serial row data (upper right half)
8	D4	H/L	Serial row data (lower right half)
9	V_{DD}	—	Power supply for logic circuit
10	V_{SS}	—	Ground
11	V_{EE}	—	Power supply for LC driving
12	V_O	—	Operating voltage for LC driving

Unit: mm

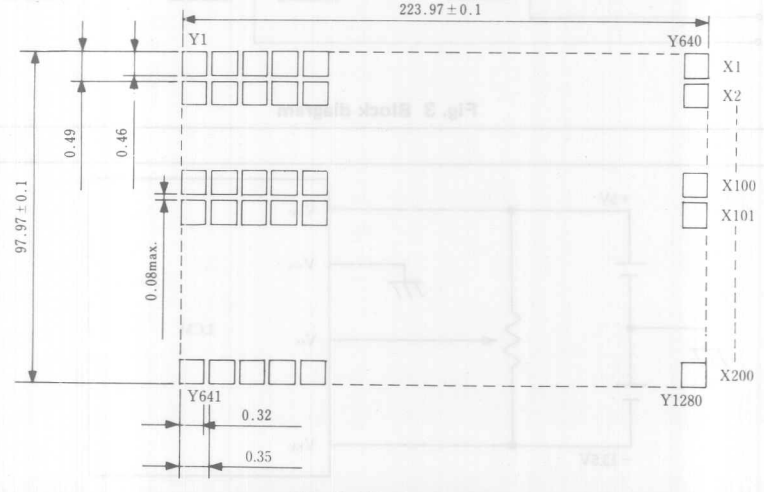


Fig. 1 Display pattern

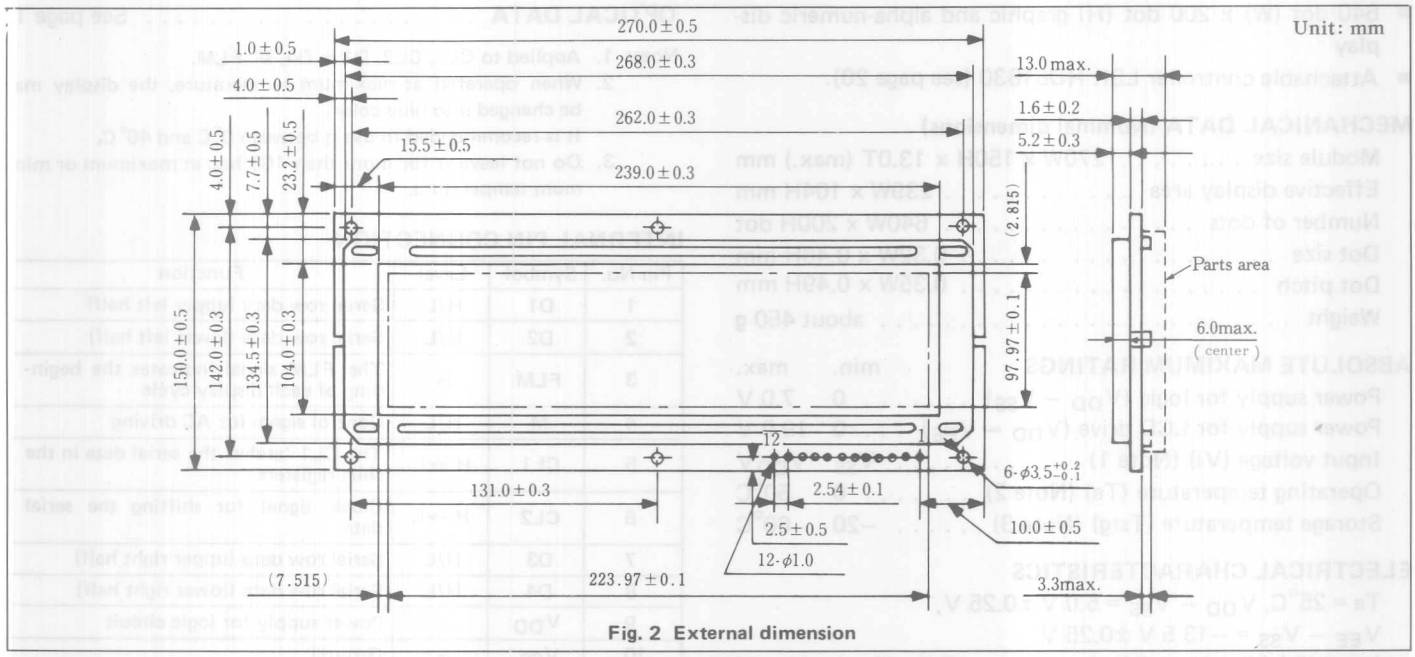


Fig. 2 External dimension

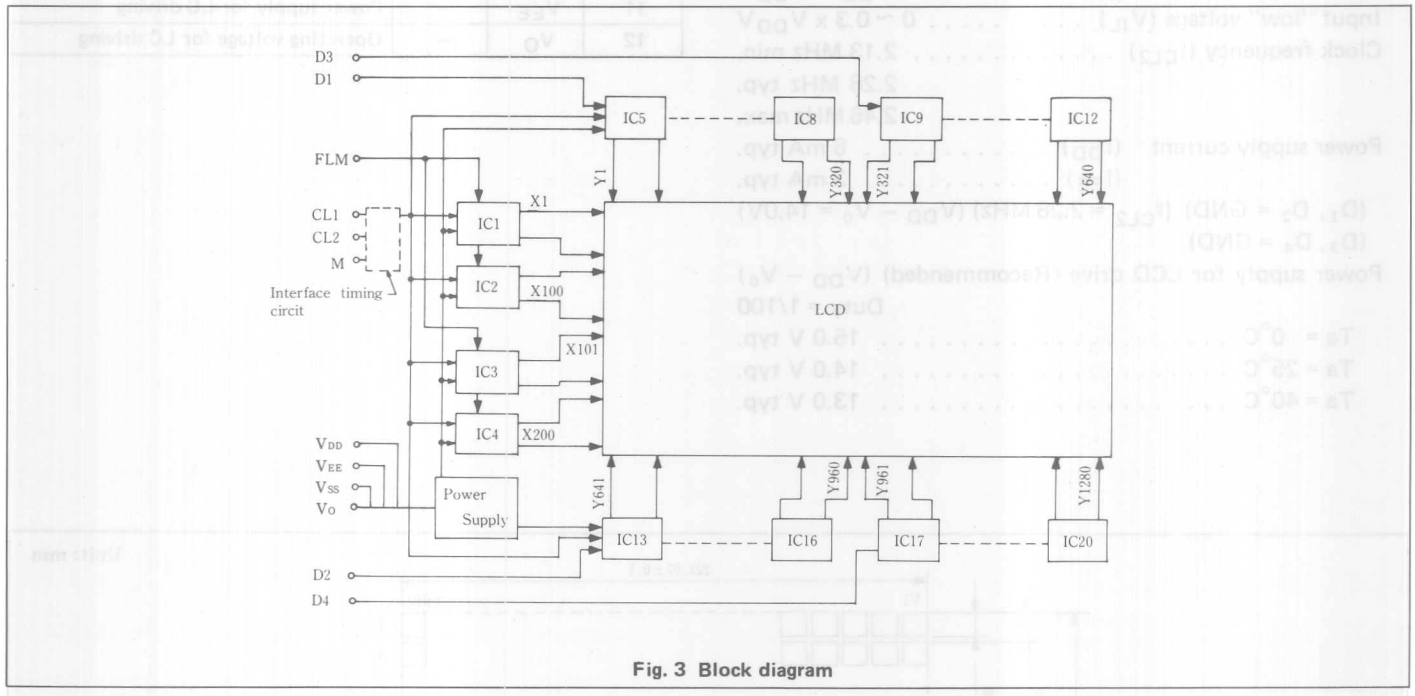


Fig. 3 Block diagram

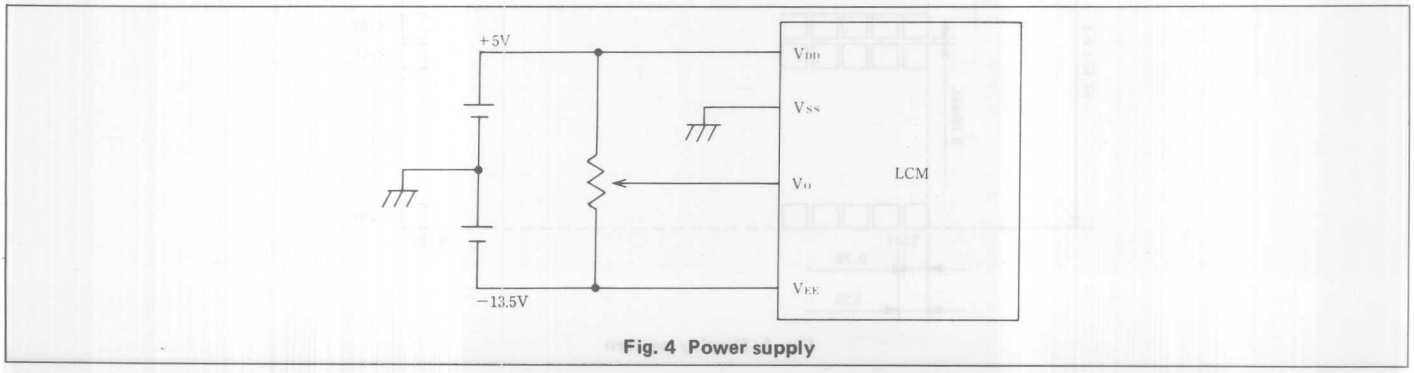


Fig. 4 Power supply

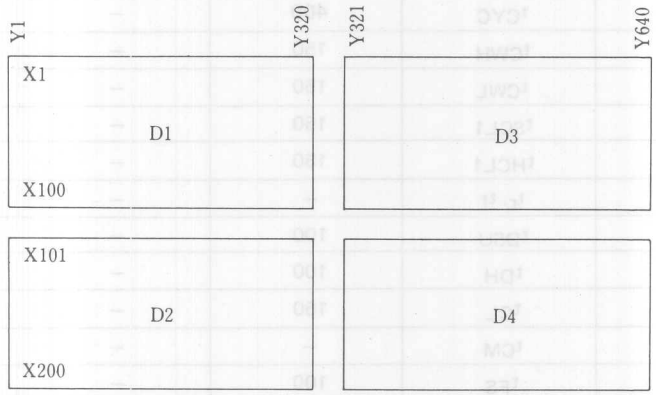


Fig. 5 Correspondence of display with data

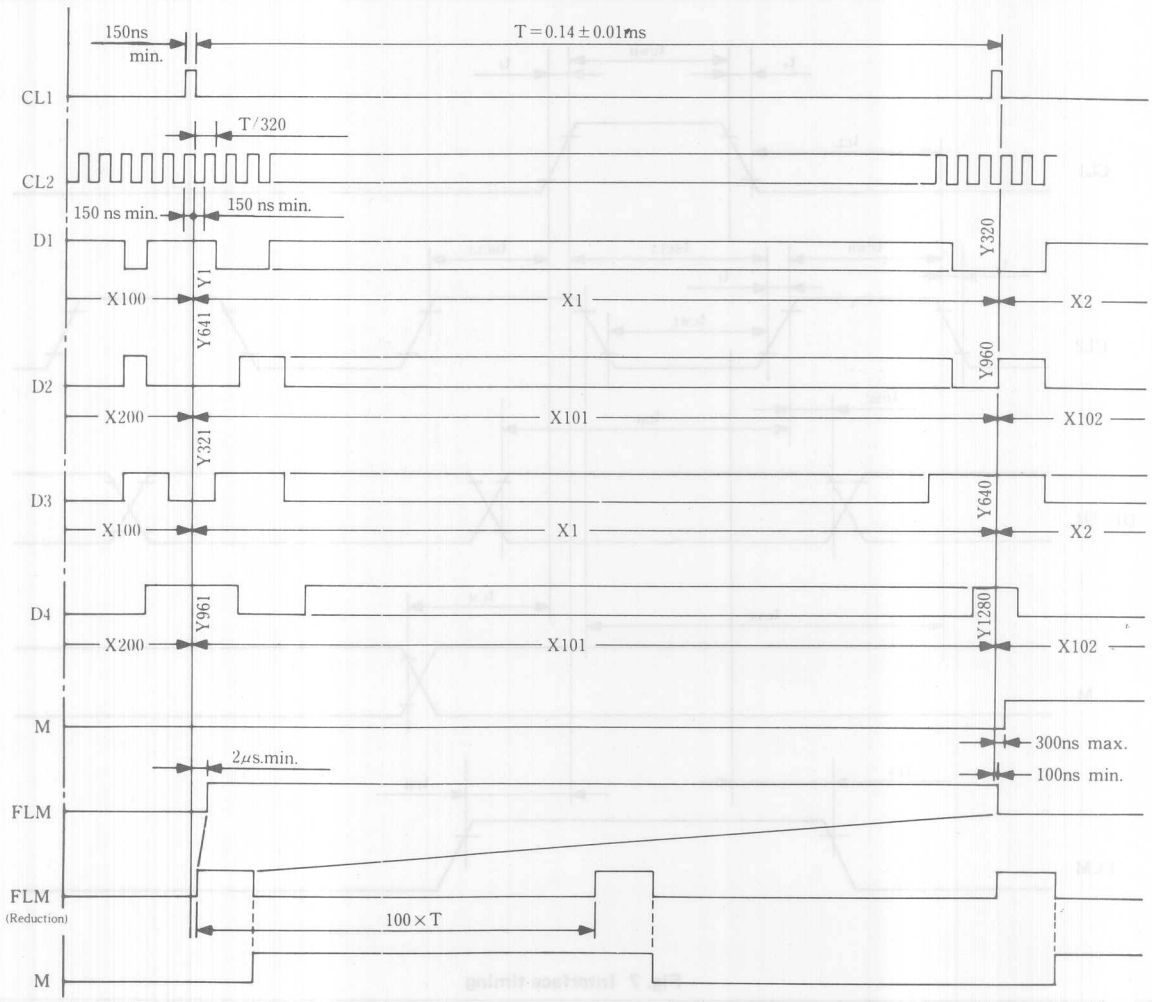


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	400	–	–	ns
CL2 pulse width (H)	t_{CWH}	150	–	–	ns
CL2 pulse width (L)	t_{CWL}	150	–	–	ns
CL1 set up time (1)	t_{SCL1}	150	–	–	ns
CL1 set up time (2)	t_{HCL1}	150	–	–	ns
Clock rise/fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
CL1 delay time	t_{CL}	150	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	100	–	–	ns
FLM hold time	t_{FH}	100	–	–	ns

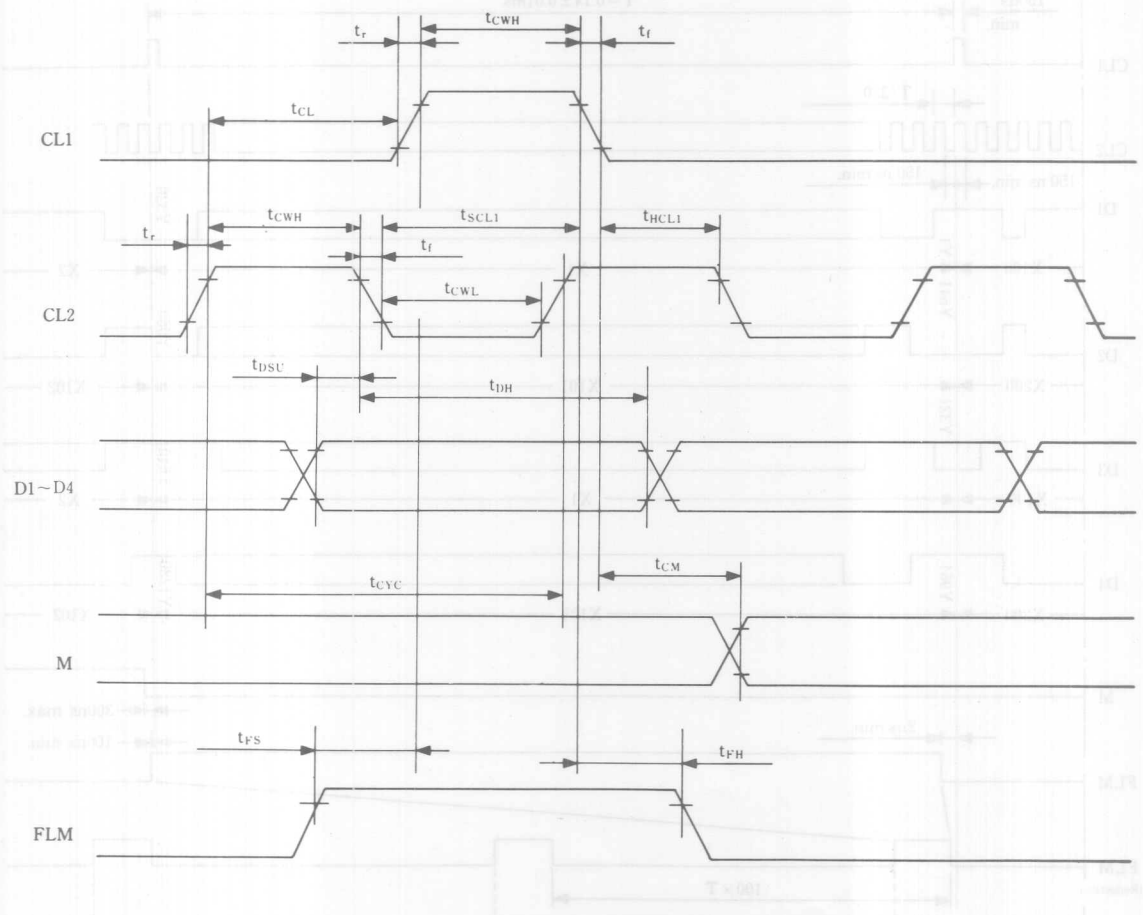


Fig. 7 Interface timing

LM240S

- 480 dot (W) x 128 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: MSM6255GSK or MSM6265GSK

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 270W x 110H x 11.5T (max.) mm
Effective display area . . . . . 242W x 69H mm
Number of dots . . . . . 480W x 128H dot
Dot size . . . . . 0.43W x 0.43H mm
Dot pitch . . . . . 0.48W x 0.48H mm
Weight . . . . . about 320 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	22 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V,
V_{EE} = −14.5 V ±0.5 V

Input "high" voltage (V_{IH}) . . . . . 0.8 x V_{DD} V min.
Input "low" voltage (V_{IL}) . . . . . 0.2 x V_{DD} V max.
Clock frequency (f_{CL2}) . . . . . 1.00 MHz min.
1.07 MHz typ.
1.15 MHz max.
Power supply current (I_{DD}) . . . . . 10 mA typ.
(I_{EE}) . . . . . 8 mA typ.
(D_1, D_2 = GND) (f_{CL2} = 1.07 MHz) ($V_{DD} - V_0$ = 15.8V)
(D_3, D_4 = GND)
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/128
Ta = 0°C . . . . . 17.1 V typ.
Ta = 25°C . . . . . 15.8 V typ.
Ta = 40°C . . . . . 14.6 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D0	H/L	Serial row data
2	D1	H/L	Serial row data
3	FRAME	H	Frame frequency (Indicating the beginning of each display cycle)
4	N.C	—	—
5	LOAD	H/L	The CL1 latches the serial data in the shift registers
6	CP	H/L	Clock signal for shifting the serial data
7	D2	H/L	Serial row data
8	D3	H/L	Serial row data
9	V_{DD}	—	Power supply for logic circuit
10	V_{SS}	—	Ground
11	V_{EE}	—	Power supply for LC driving
12	V_0	—	Operating voltage for LC driving
13	ECLK	H/L	Enable clock
14	N.C	—	—
15	N.C	—	—

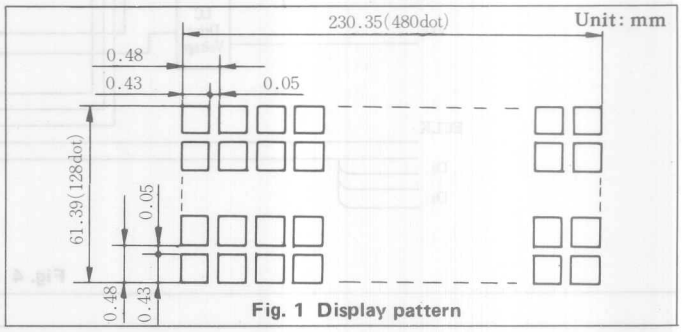


Fig. 1 Display pattern

Unit: mm

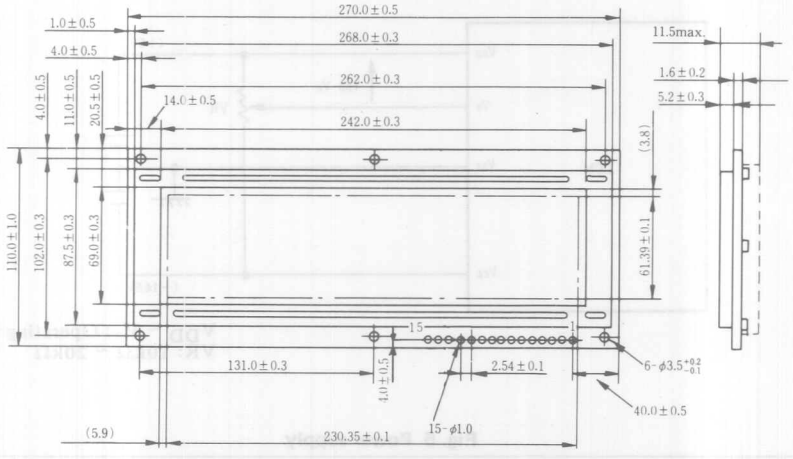


Fig. 2 External dimension

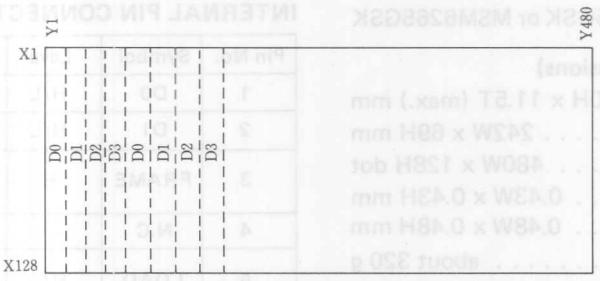


Fig. 3 Correspondence of display with data

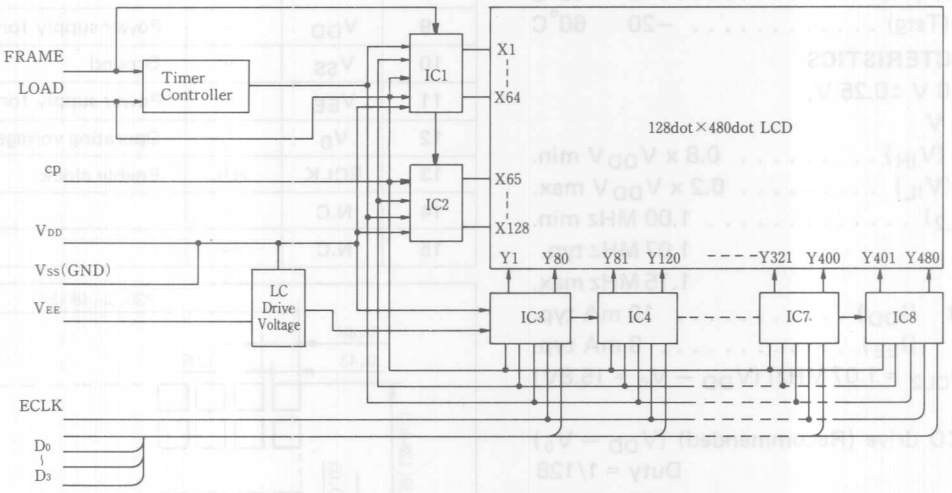
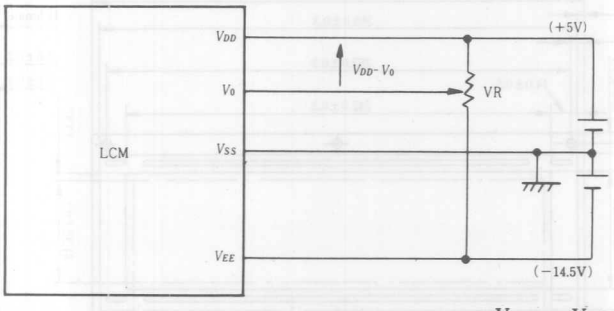
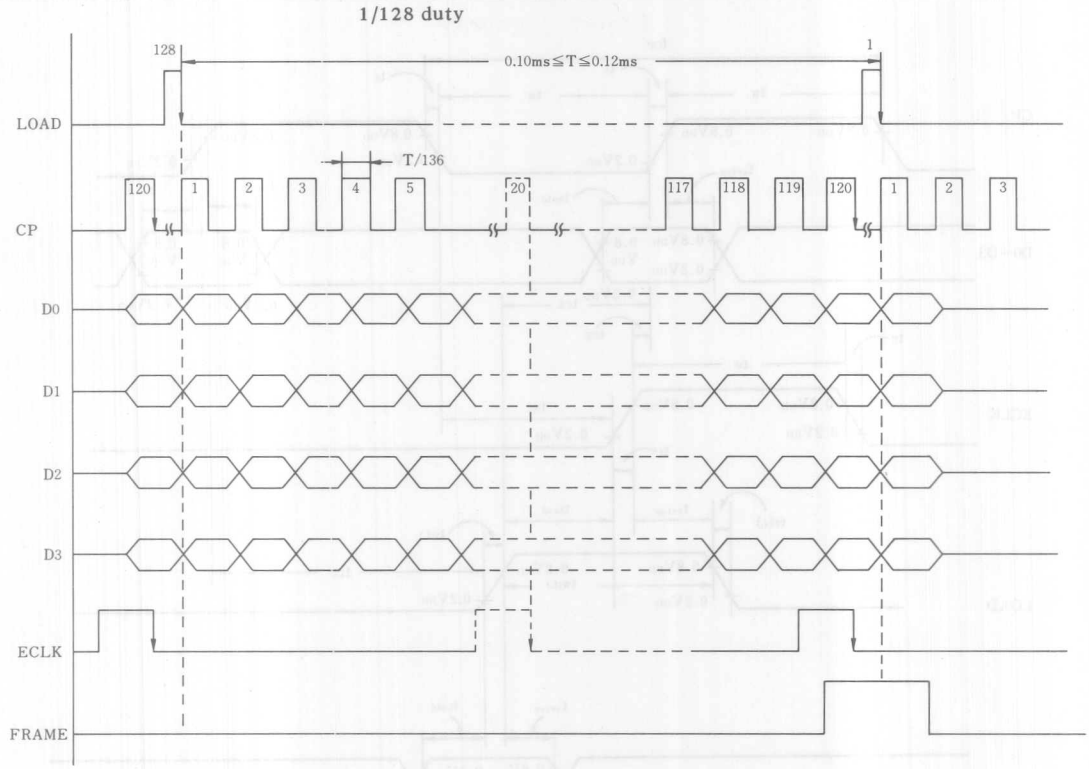


Fig. 4 Block diagram



$V_{DD} \sim V_0$: Operating voltage for LC driving
VR: 10kΩ ~ 20kΩ

Fig. 5 Power supply



Notes 1. When using control LSI MSM6255GSK.
2. There is CP pulse interrupting time of sixteen pulses between CP (120) and CP (1).

Fig. 6 Interface timing

TIMING CHARACTERISTICS

(V_{DD} = 5V ±10%, Ta = −20 ~ +85°C, CL = 15μF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" delay time	t_{PLH} t_{PHL}	–	–	–	200	ns
Maximum clock frequency	f_{CP}	DUTY = 50%	–	–	1.3	MHz
CP ECLK pulse width	t_W	–	125	–	–	ns
LOAD pulse width	$t_{W\,(L)}$	–	125	–	–	ns
Set up time	t_{setup}	–	100	–	–	ns
CP → LOAD time	t_{CL}	–	250	–	–	ns
LOAD → CP time	t_{LC}	–	0	–	–	ns
Hold time	t_{hold}	–	100	–	–	ns
Rise, fall time	t_r t_f	–	–	–	50	ns
LOAD rise, fall time	$t_{r\,(L)}$ $t_{f\,(L)}$	–	–	–	1	μs
CP → ECLK time	t_{CE}	–	0	–	–	ns
ECLK → CP time	t_{EC}	–	150	–	–	ns

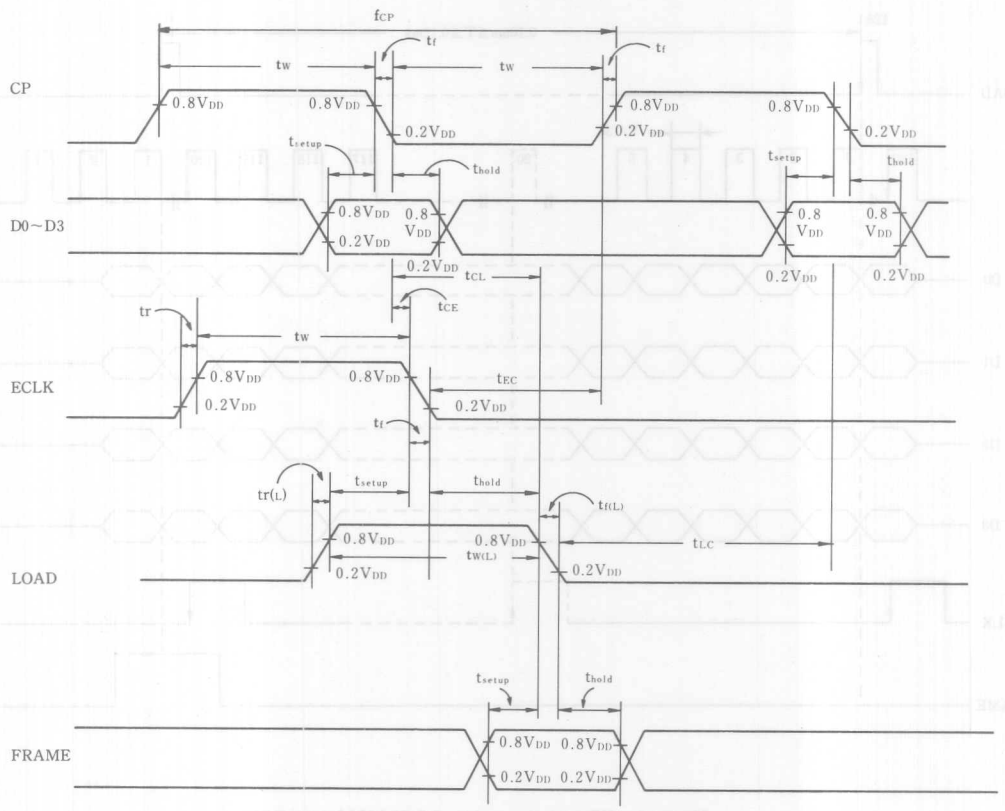


Fig. 7 Interface timing

LM236SB

- 640 dot (W) x 200 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: MSM6255GSK or MSM6265GSK

MECHANICAL DATA (Nominal dimensions)

Module size	270W x 149H x 13.0T (max.) mm
Effective display area	239W x 104H mm
Number of dots	640W x 200H dot
Dot size	0.32W x 0.46H mm
Dot pitch	0.35W x 0.49H mm
Weight	about 450 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic (V_{DD})	0	6.5 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	22 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD} + 0.3 V
Operating temperature (Ta) (Note 2)	0	50°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V,
V_{EE} = −14.5 V ±0.5 V

Input "high" voltage (V_{IH}) (Note 1)	0.8 x V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL}) (Note 1)	0 ~ 0.2 x V_{DD} V
Power supply current (I_{DD}) (Note 4)	5 mA typ.
(I_{EE}) (Note 4)	4 mA typ.
Frame frequency (f_{FRAME})	70 Hz min.
	75 Hz typ.
	80 Hz max.
Input capacitance (C_{in}) (f_{CP} = 1 MHz)	150 pF typ.
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$) (Note 5)	Duty = 1/100
Ta = 0°C	16.0 V typ.
Ta = 25°C	15.0 V typ.
Ta = 40°C	14.0 V typ.

OPTICAL DATA

See page 11

Notes 1. Applied to FRAME, LOAD, DF, ECLK, CP, UD0 ~ UD3, LD0 ~ LD3.
2. When operated at maximum temperature, the display may change into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.
4. When viewing angle is 25°.
5. In case of V_{DD} = +5V, $V_{DD} - V_0$ = 15V, DF = 75 Hz, UD0 ~ UD3 = V_{SS} and LD0 ~ LD3 = V_{SS}.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1 ~ 4	UD0 ~ UD3	H/L	Data (upper half)
5	ECLK	H	Chip enable clock
6	FRAME	H	Frame frequency (Indicating the beginning of each display cycle)
7	DF	H/L	Control signal for AC driving
8	LOAD	H → L	Data latch
9	CP	H → L	Data shift
10 ~ 13	LD0 ~ LD3	H/L	Data (lower half)
14	V_{DD}	—	Power supply for logic circuit
15	V_{SS}	—	Ground
16	V_{EE}	—	Power supply for LC driving
17	V_0	—	Operating voltage for LC driving

Unit: mm

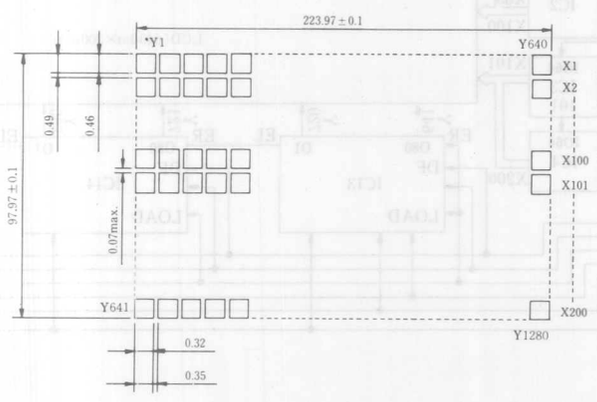
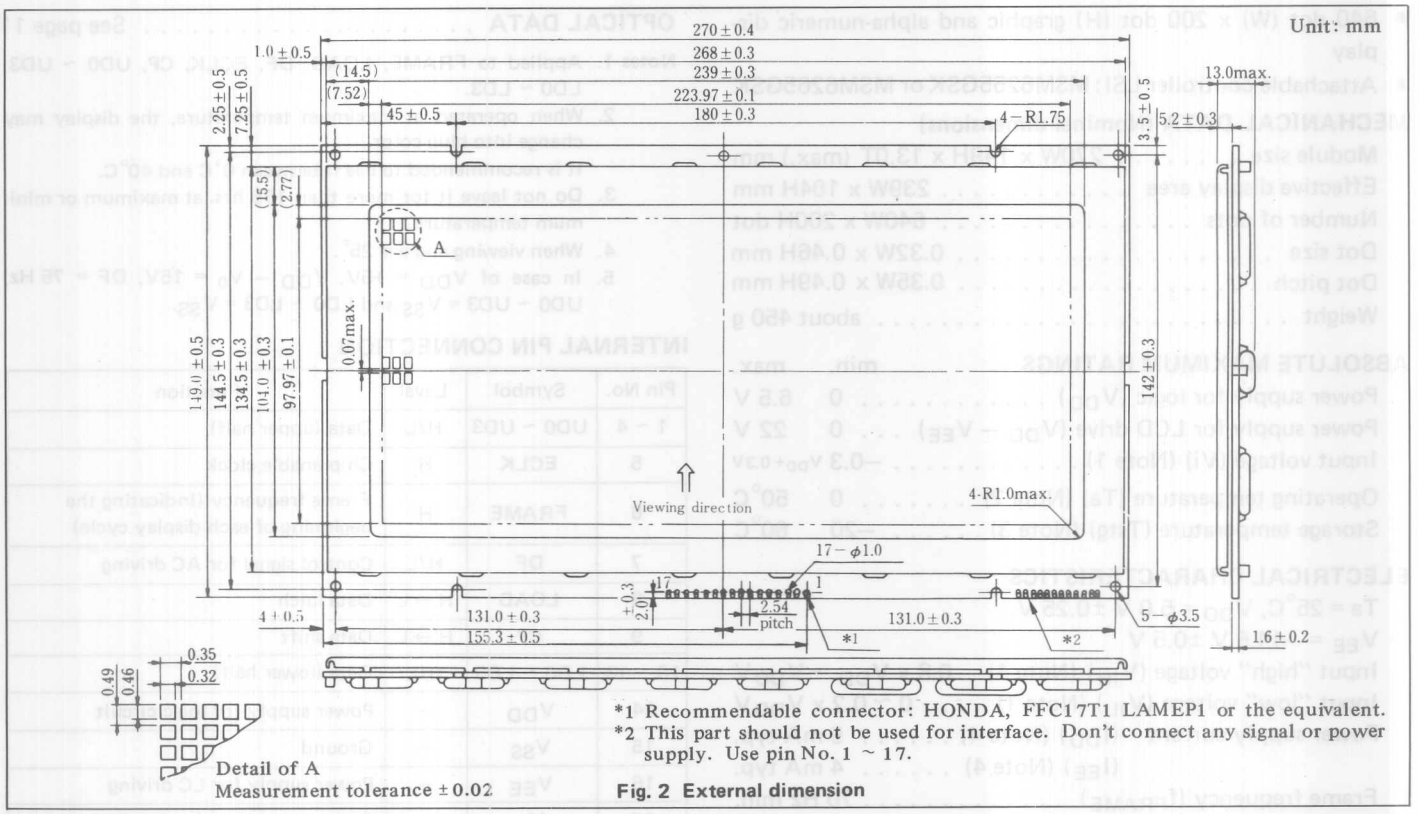


Fig. 1 Display pattern



*1 Recommendable connector: HONDA, FFC17T1 LAMEP1 or the equivalent.
*2 This part should not be used for interface. Don't connect any signal or power supply. Use pin No. 1 ~ 17.

Fig. 2 External dimension

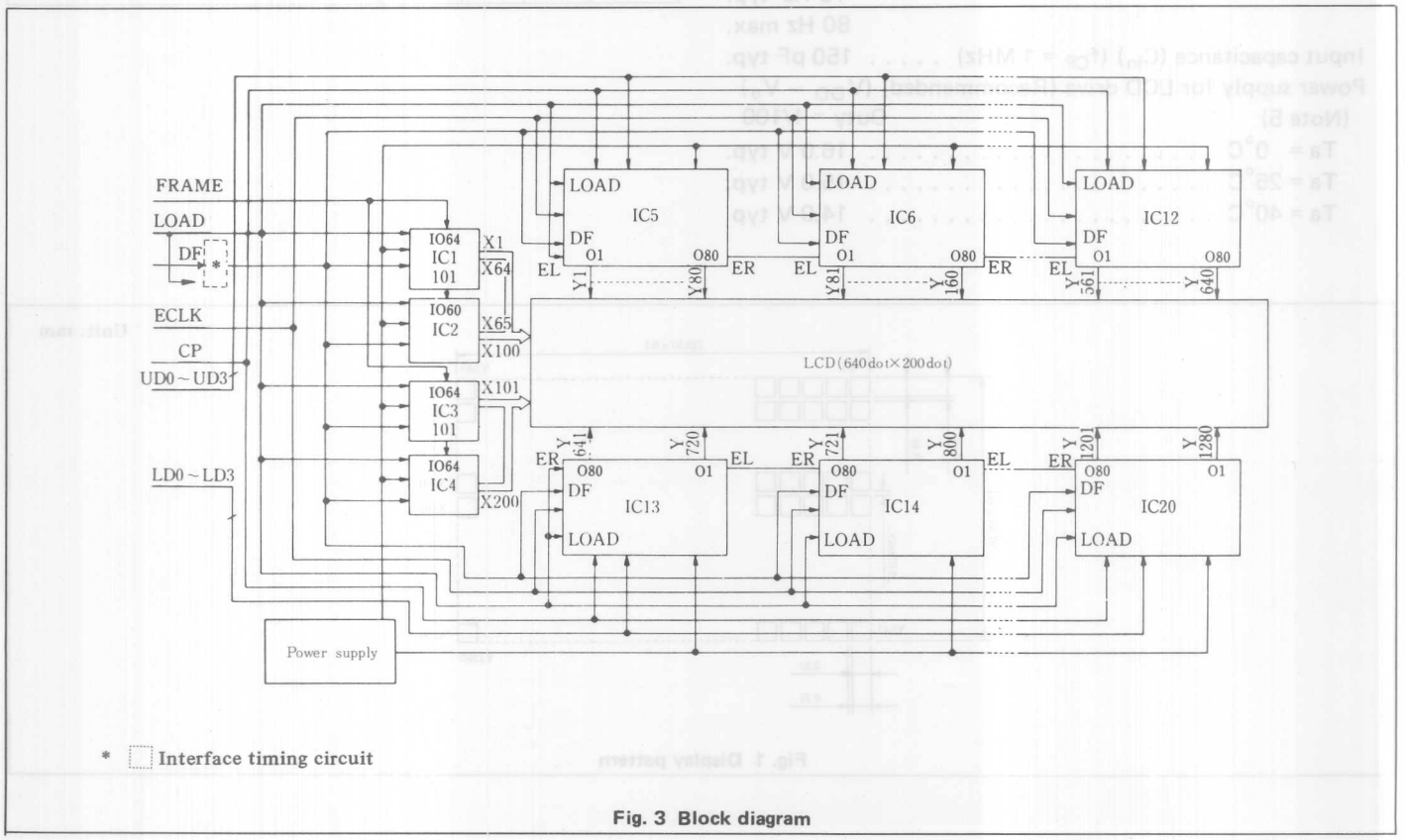
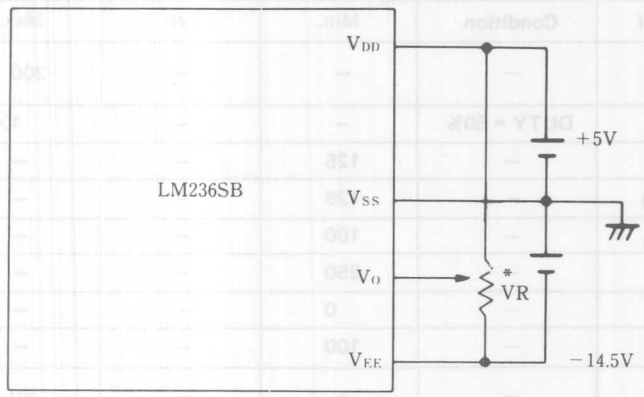
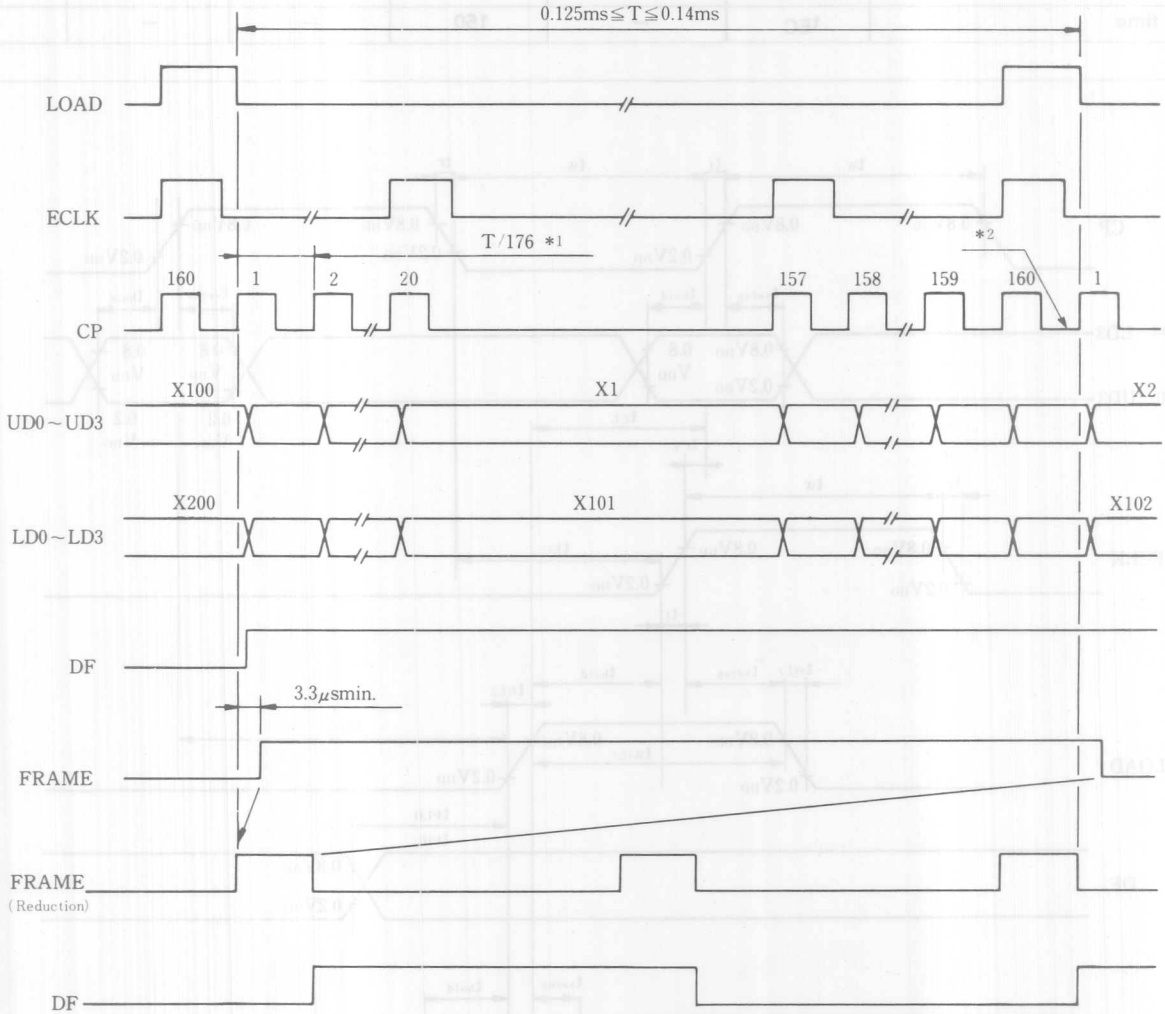


Fig. 3 Block diagram



* VR: 10kΩ ~ 20kΩ

Fig. 4 Power supply



*1 When using control LSI MSM6255GSK.
*2 There is CP pulse interrupting time of sixteen pulse between CP (160) and CP (1).

Fig. 5 Interface timing

TIMING CHARACTERISTICS

(V_{DD} = 5V ±10%, Ta = −20 ~ +85°C, CL = 15 μF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" delay time	t_{PLH} t_{PHL}	–	–	–	200	ns
Frequency of maximum clock	f_{CP}	DUTY = 50%	–	–	1.41	MHz
CP ECLK pulse width	t_W	–	125	–	–	ns
LOAD pulse width	t_W (L)	–	125	–	–	ns
Set up time	t_{setup}	–	100	–	–	ns
CP → LOAD time	t_{CL}	–	250	–	–	ns
LOAD → CP time	t_{LC}	–	0	–	–	ns
Hold time	t_{hold}	–	100	–	–	ns
Rise, Fall time	t_r t_f	–	–	–	50	ns
LOAD rise, fall time	t_r (L) t_f (L)	–	–	–	1	μs
CP → ECLK time	t_{CE}	–	0	–	–	ns
ECLK → CP time	t_{EC}	–	150	–	–	ns

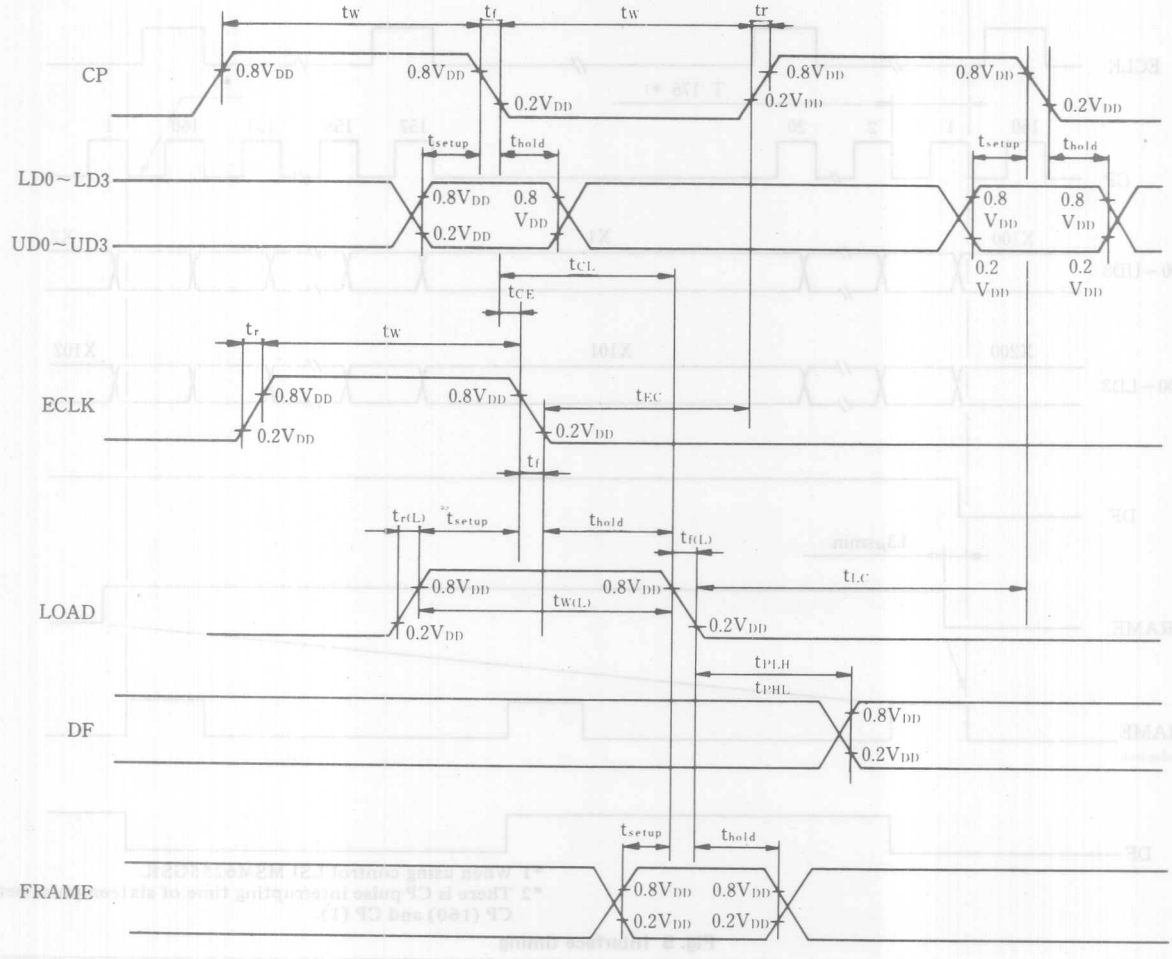


Fig. 6 Interface timing

LM585S

- 640 dot (W) x 200 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: MSM6255GSK or MSM6265GSK

MECHANICAL DATA (Nominal dimensions)

Module size	260W x 195H x 12.5T (max.) mm
Effective display area	220W x 166H mm
Number of dots	640W x 200H dot
Dot size	0.29W x 0.74H mm
Dot pitch	0.32W x 0.77H mm
Weight	about 540 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic (V_{DD})	0	6.5 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	22 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD}+ 0.3V
Operating temperature (Ta) (Note 2)	0	50°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V,
$V_{DD} - V_{EE}$ = 19.5 V ±0.5 V

Input "high" voltage (V_{IH})	0.8 x V_{DD}V min.
Input "low" voltage (V_{IL})	0.2 x V_{DD}V max.
Power supply current (I_{DD}) (Note 4)	5 mA typ.
(I_{EE}) (Note 4)	4 mA typ.
Frame frequency (f_{FRAME})	70 Hz min.
	75 Hz typ.
	80 Hz max.
Input capacitance (C_{in}) (f_{CP} = 1 MHz)	150 pF typ.
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$) (Note 5)	Duty = 1/100
Ta = 0°C	16.0 V typ.
Ta = 25°C	15.0 V typ.
Ta = 40°C	14.0 V typ.

OPTICAL DATA

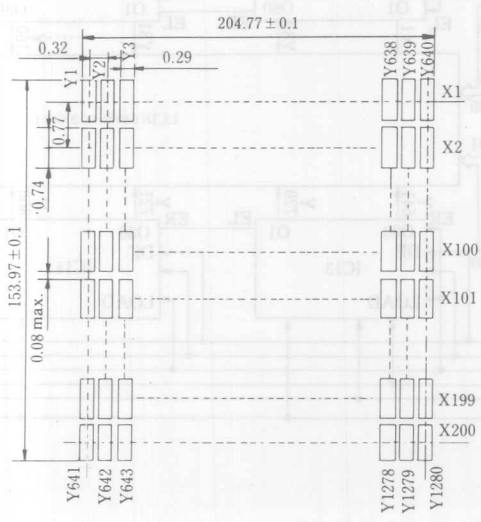
See page 11

Notes 1. Applied to FRAME, LOAD, DF, ECLK, CP, UD0 ~ UD3, LD0 ~ LD3.
2. When operated at maximum temperature, the display may change into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.
4. When viewing angle is 25°C.
5. In case of V_{DD} = +5V, $V_{DD} - V_0$ = 15V, DF = 75 Hz, UD0 ~ UD3 = 0V and LD0 ~ LD3 = 0V.

INTERNAL PIN CONNECTION

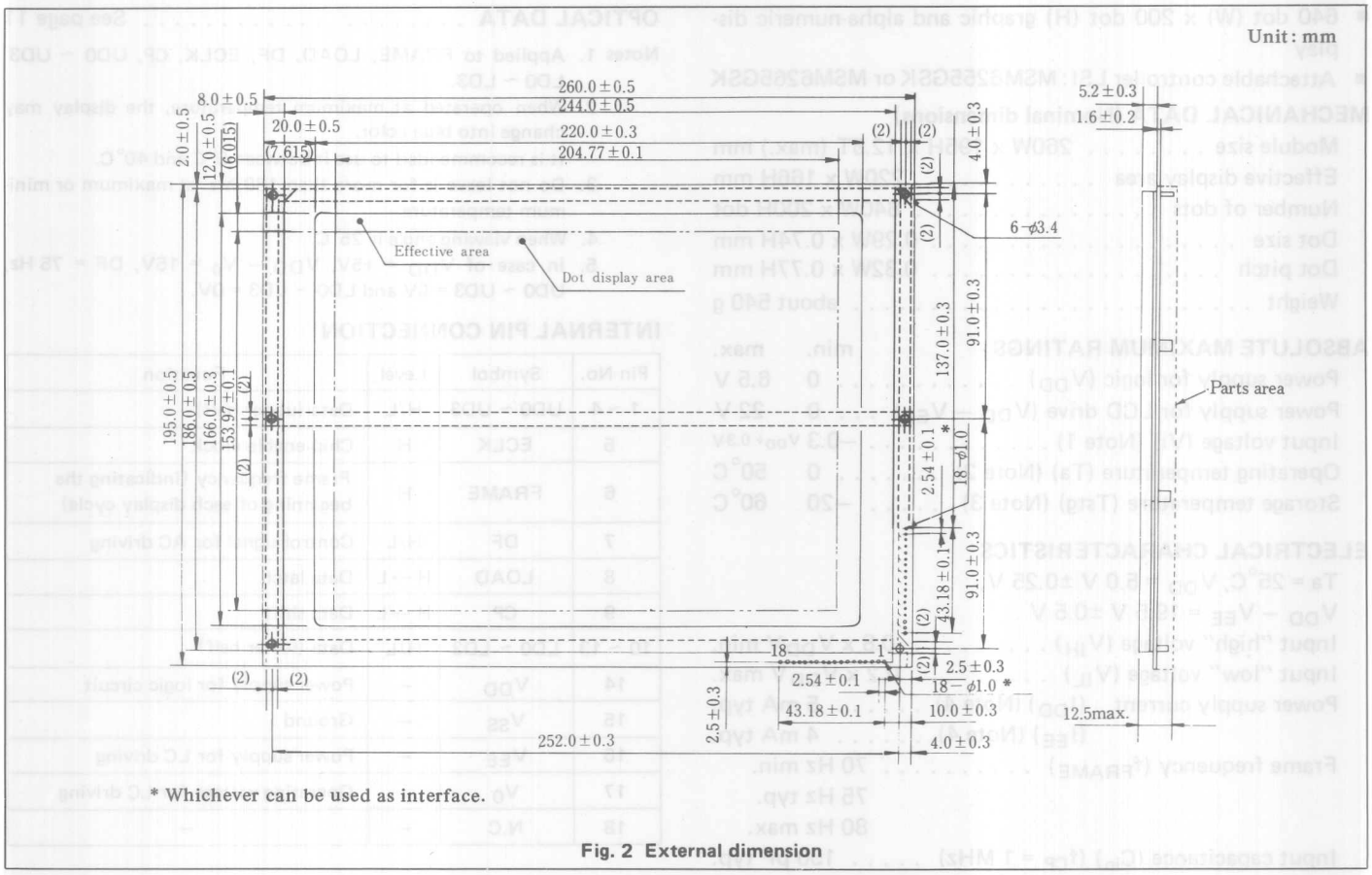
Pin No.	Symbol	Level	Function
1 ~ 4	UD0 ~ UD3	H/L	Data (upper half)
5	ECLK	H	Chip enable clock
6	FRAME	H	Frame frequency (Indicating the beginning of each display cycle)
7	DF	H/L	Control signal for AC driving
8	LOAD	H → L	Data latch
9	CP	H → L	Data shift
10 ~ 13	LD0 ~ LD3	H/L	Data (lower half)
14	V_{DD}	–	Power supply for logic circuit
15	V_{SS}	–	Ground
16	V_{EE}	–	Power supply for LC driving
17	V_0	–	Operating voltage for LC driving
18	N.C	–	–

Unit: mm



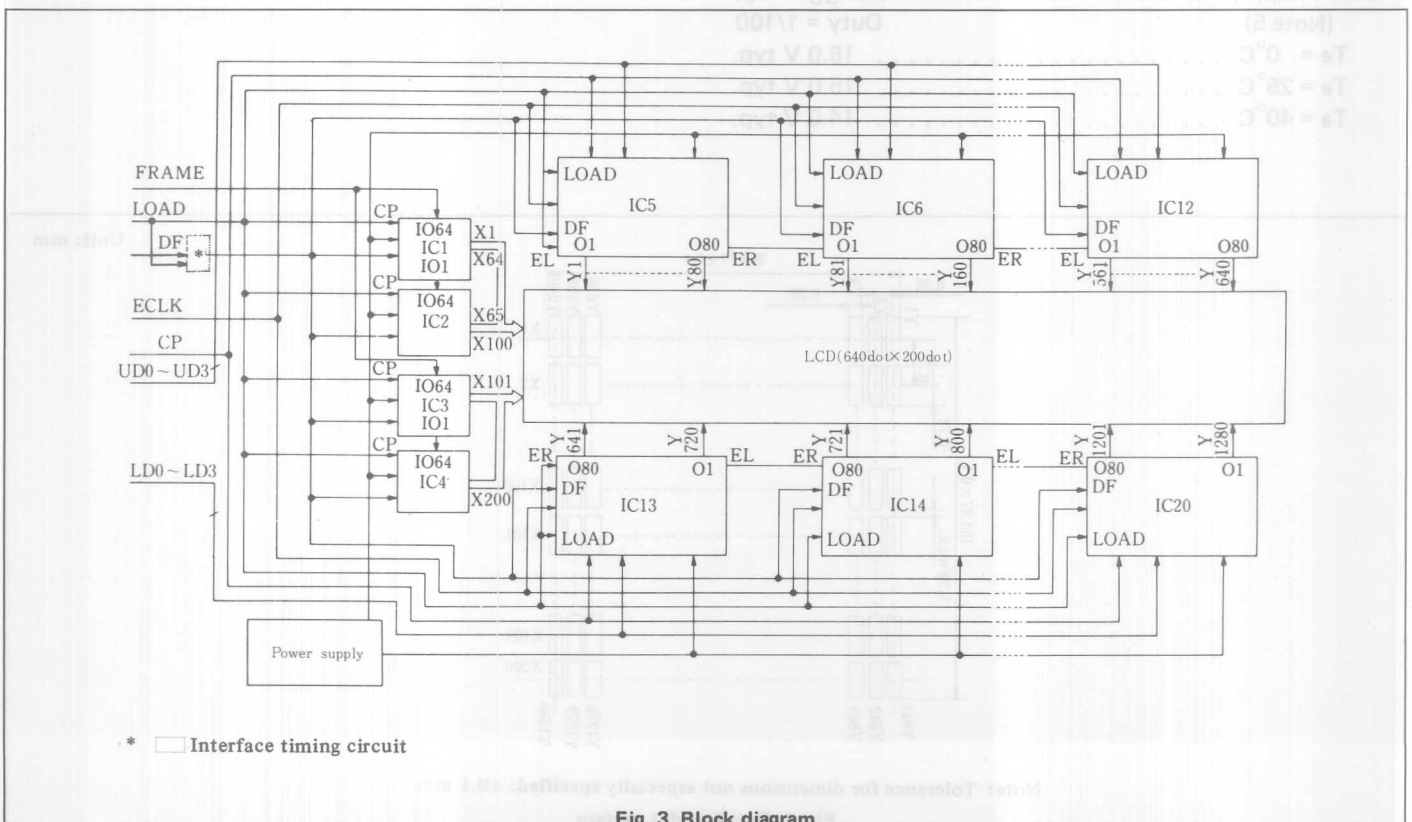
Note: Tolerance for dimensions not especially specified: ±0.1 mm

Fig. 1 Detail of dot pattern



* Whichever can be used as interface.

Fig. 2 External dimension



* Interface timing circuit

Fig. 3 Block diagram

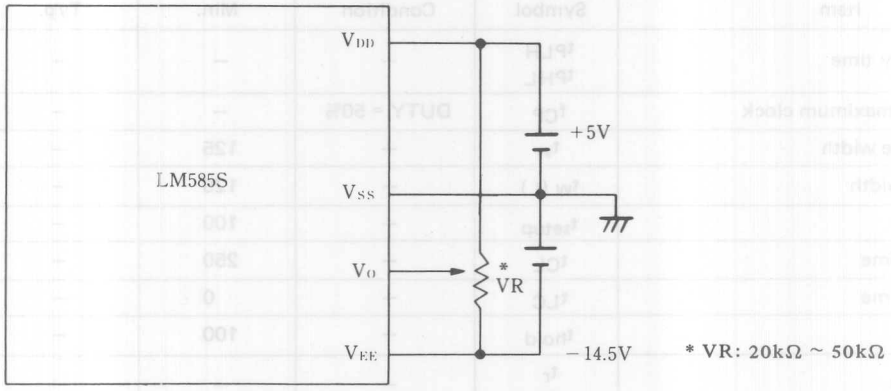
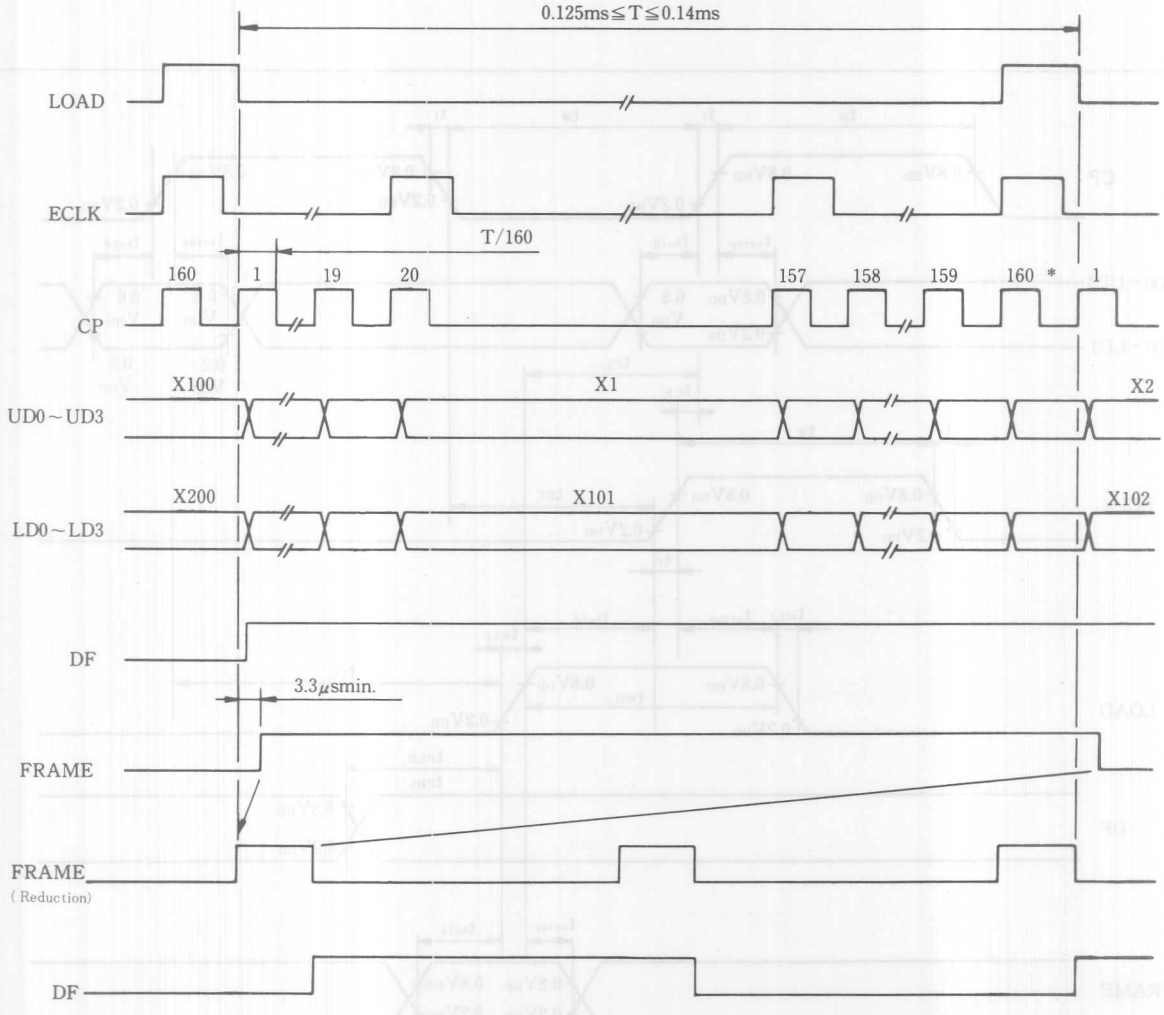


Fig. 4 Power supply



* There is CP pulse interrupting time of sixteen pulse between CP (160) and CP (1).

Fig. 5 Interface timing

TIMING CHARACTERISTICS

(V_{DD} = 5V ±10%, Ta = −20 ~ +85° C, CL = 15 μF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" delay time	t_{PLH} t_{PHL}	–	–	–	200	ns
Frequency of maximum clock	f_{CP}	DUTY = 50%	–	–	1.41	MHz
CP ECLK pulse width	t_w	–	125	–	–	ns
LOAD pulse width	$t_{w(L)}$	–	125	–	–	ns
Set up time	t_{setup}	–	100	–	–	ns
CP → LOAD time	t_{CL}	–	250	–	–	ns
LOAD → CP time	t_{LC}	–	0	–	–	ns
Hold time	t_{hold}	–	100	–	–	ns
Rise, Fall time	t_r t_f	–	–	–	50	ns
LOAD rise, fall time	$t_{r(L)}$ $t_{f(L)}$	–	–	–	1	μs
CP → ECLK time	t_{CE}	–	0	–	–	ns
ECLK → CP time	t_{EC}	–	150	–	–	ns

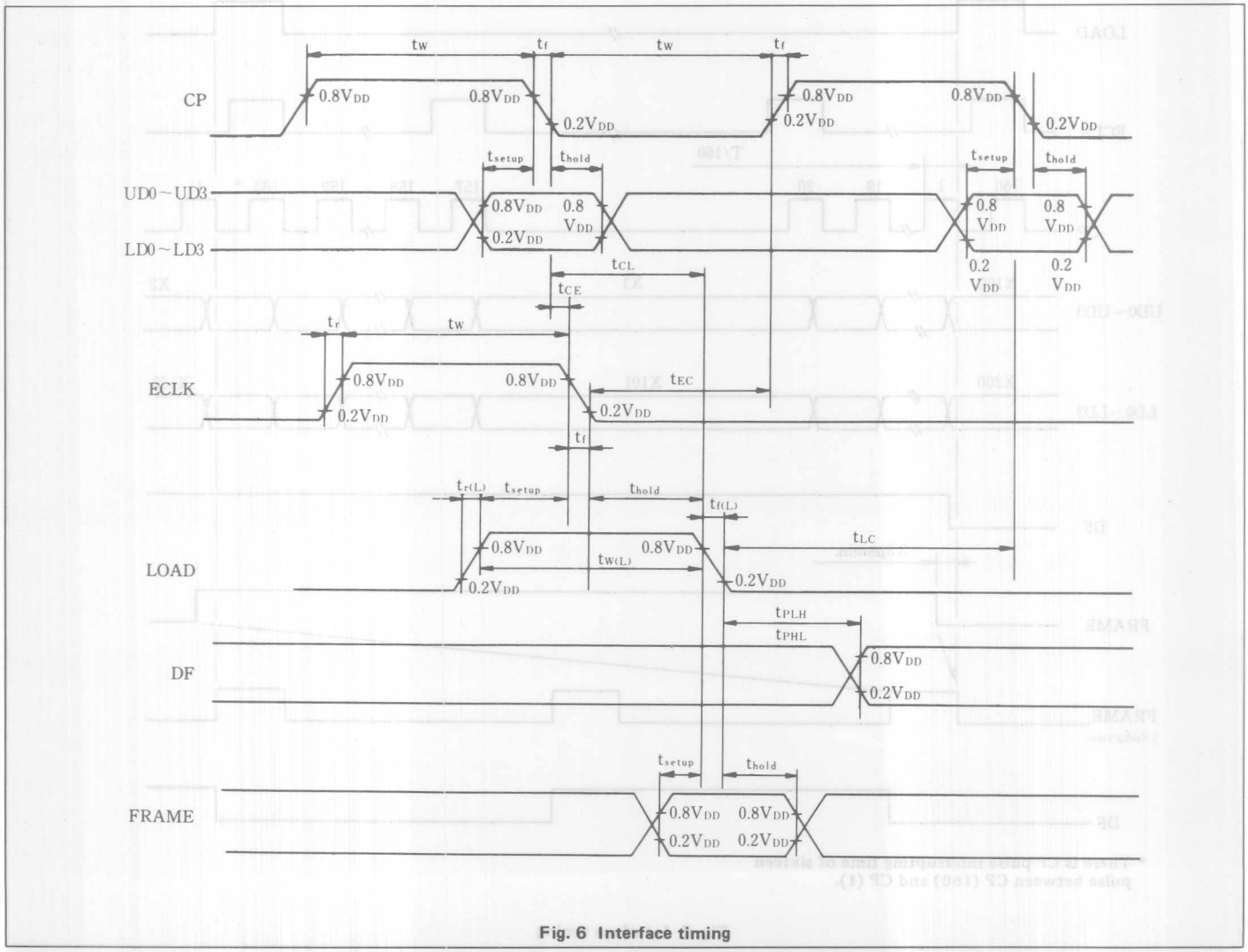


Fig. 6 Interface timing

LCD MODULE WITH BUILT-IN CONTROLLER LSI

This is a dot matrix LCD module containing the controller LSI HD44780 (LCD-II) for character display. Functions such as control, refresh, and display are operated by the built-in controller LSI, HD44780 (LCD-II).

This LCD module can display 160 type JIS characters and symbols and 32 type special characters and symbols. This LCD module can be interfaced to the 4-bit or 8-bit MPU, so the character display and the display shift can be easily operated by using control commands. This LCD module also contains the character generator RAM, hence user's patterns can be displayed.

Controller LSI HD44780 (LCD-II)

LM054	(8 x 1 line)	LM058	(40 x 1 line)
H2570	(16 x 1 line)	LM052L	(16 x 2 lines)
LM015	(16 x 1 line)	LM016L	(16 x 2 lines)
LM568AF	(16 x 1 line)	LM032L	(20 x 2 lines)
LM020L	(16 x 1 line)	LM060L	(24 x 2 lines)
LM070L	(20 x 1 line)	LM017L	(32 x 2 lines)
LM038	(20 x 1 line)	LM018L	(40 x 2 lines)
LM027	(24 x 1 line)	LM041L	(16 x 4 lines)
H2571	(32 x 1 line)	LM044L	(20 x 4 lines)
H2572	(40 x 1 line)		

LM054

- 8 character x 1 line
- Controller LSI HD44780 is built-in (see page 151).
- +5 V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	84W x 44H x 12D (max.) mm
Effective display area	61W x 15.8H mm
Character size (5 x 7 dots)	6.45W x 9.4H mm
Character pitch	7.15 mm
Dot size	1.25W x 1.3H mm
Weight	about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ. 2.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$) Duty = 1/8	
Ta = 0°C	4.2 V typ.
Ta = 25°C	3.7 V typ.
Ta = 50°C	3.2 V typ.

OPTICAL DATA See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4 ~ DB_7 and DB_0 ~ DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4 ~ DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0 ~ DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0 ~ DB_7.

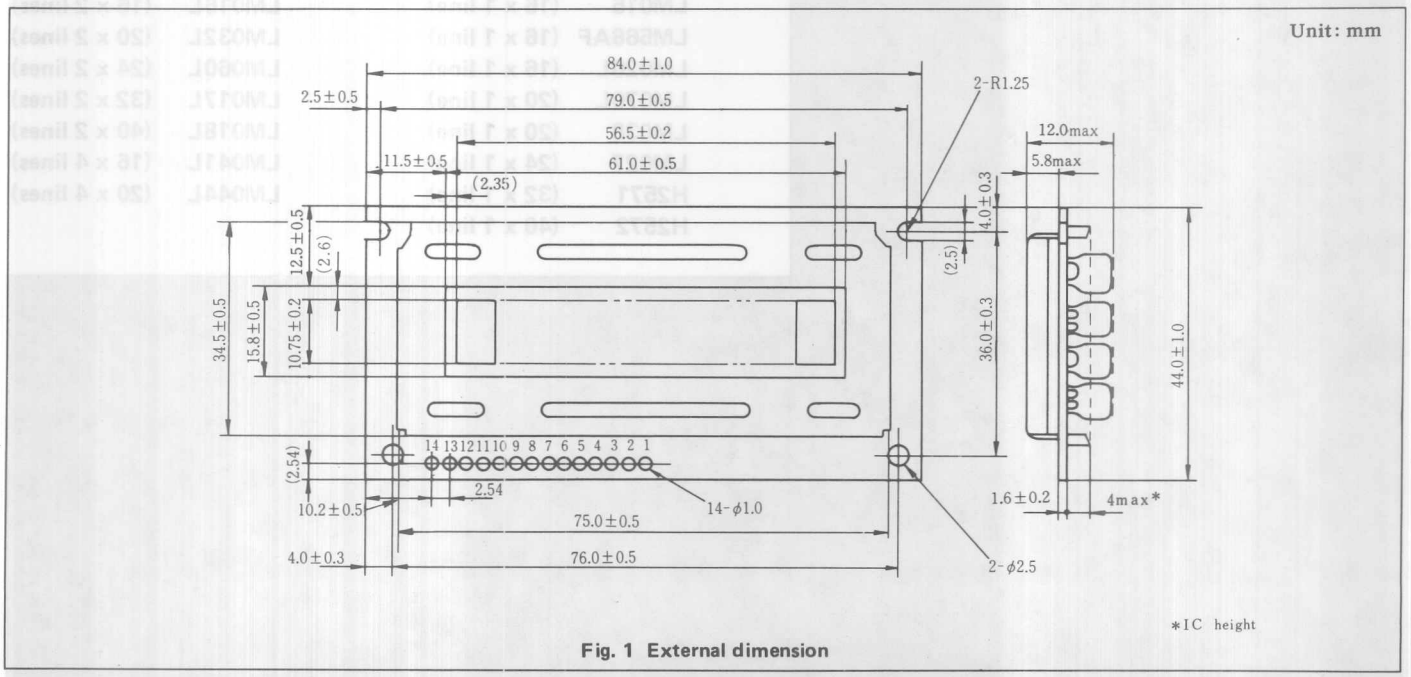


Fig. 1 External dimension

Unit: mm

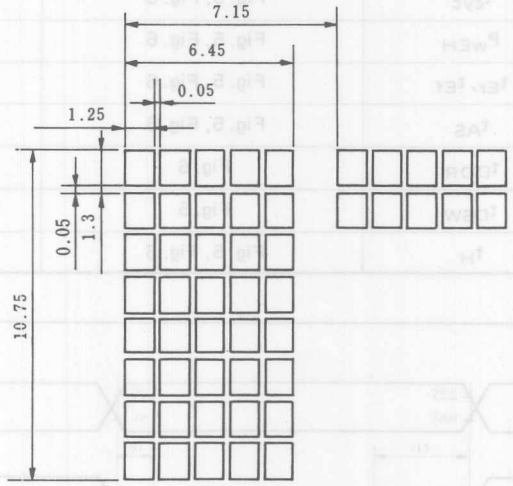


Fig. 2 Display pattern

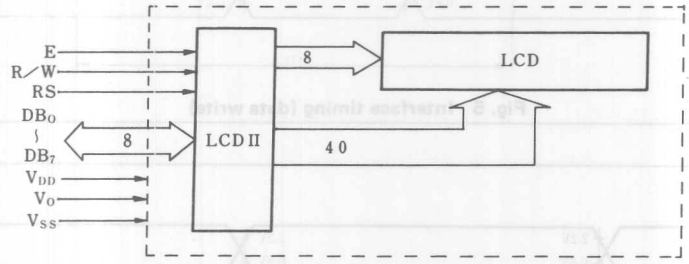
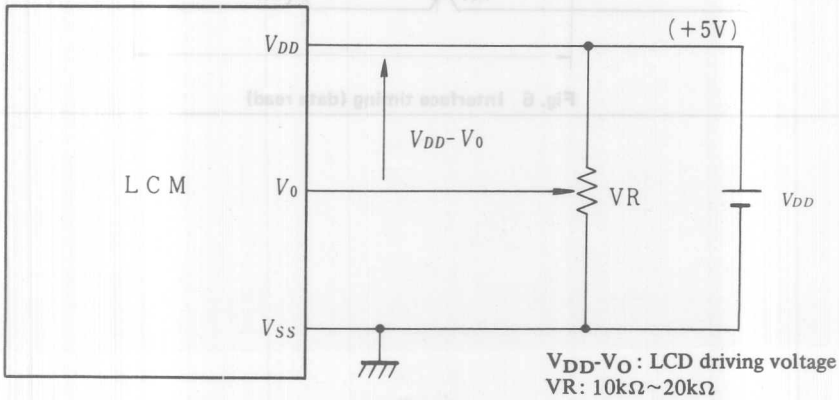


Fig. 3 Block diagram



V_{DD}-V_O : LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

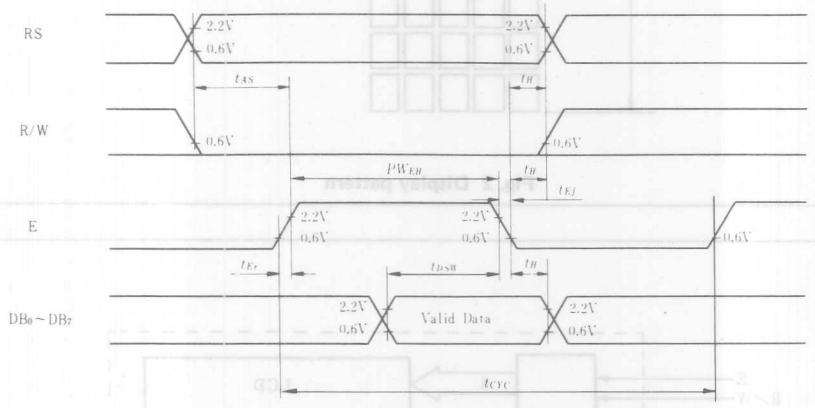


Fig. 5 Interface timing (data write)

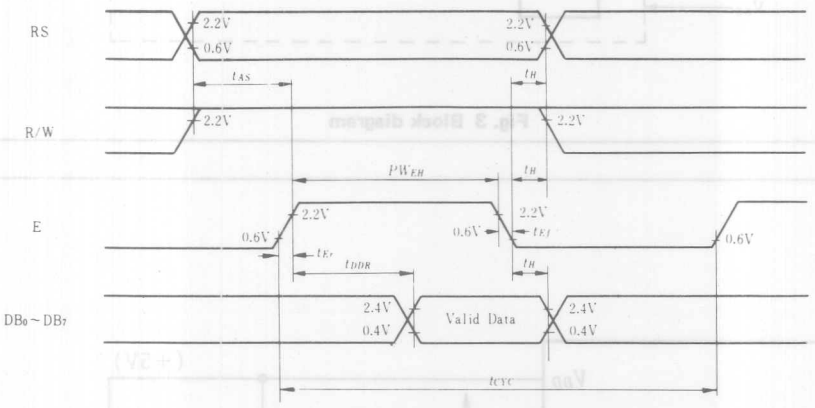


Fig. 6 Interface timing (data read)

H2570

- 16 character x 1 line
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	80W x 36H x 12D (max) mm
Effective display area	64.5W x 13.8H mm
Character size (5 x 10 dots)	3.15W x 7.9H mm
Character pitch	3.75 mm
Dot size	0.55W x 0.7H mm
Weight	about 25g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltag (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTRISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.	
Input "low" voltage (Vi_L)	0.6 V max.	
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.	
Output low voltage (V_{OL}) (I_{OL} = 1.6 mA)	0.4 V max.	
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	0.5 mA typ.	
	2.0 mA max.	

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

	Duty = 1/8	Duty = 1/11
Ta = 0°C	3.95	4.15 V typ.
Ta = 25°C	3.7	3.8 V typ.
Ta = 50°C	3.3	3.3 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	—	0V	Power supply
2	V_{DD}	—	+5V	
3	V_O	—	—	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

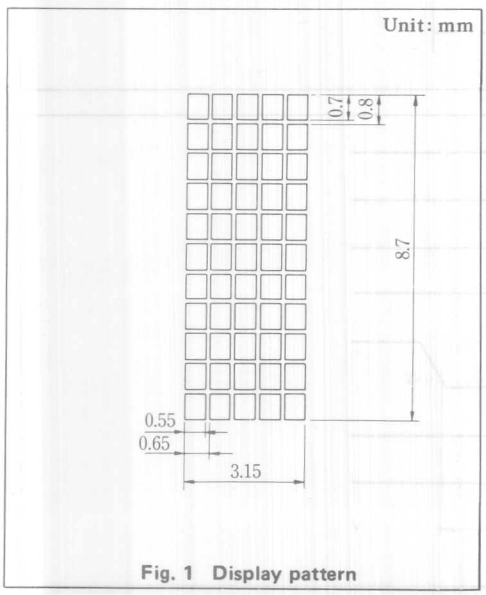


Fig. 1 Display pattern

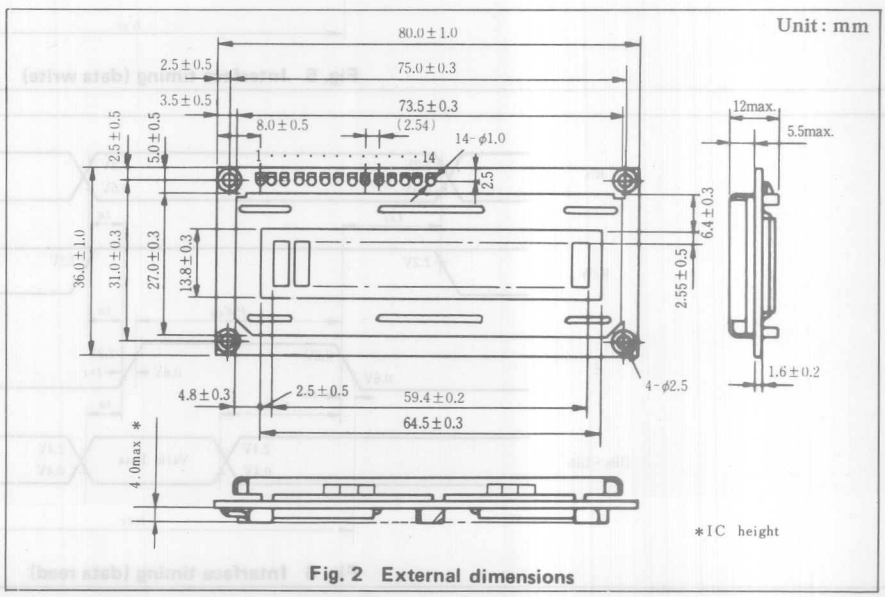


Fig. 2 External dimensions

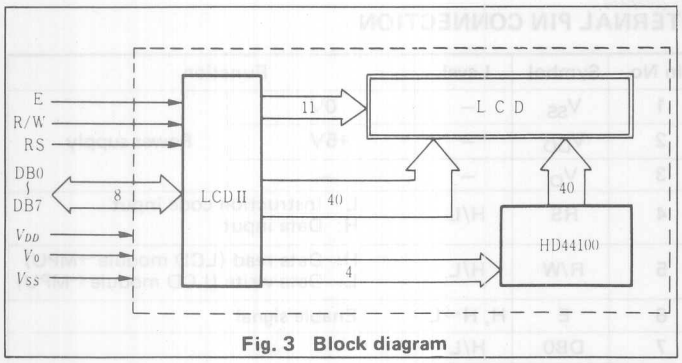


Fig. 3 Block diagram

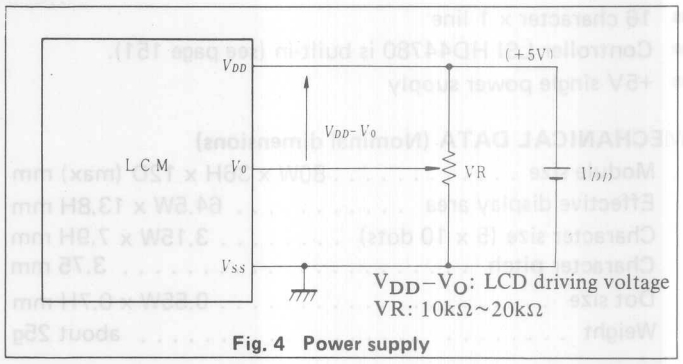


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

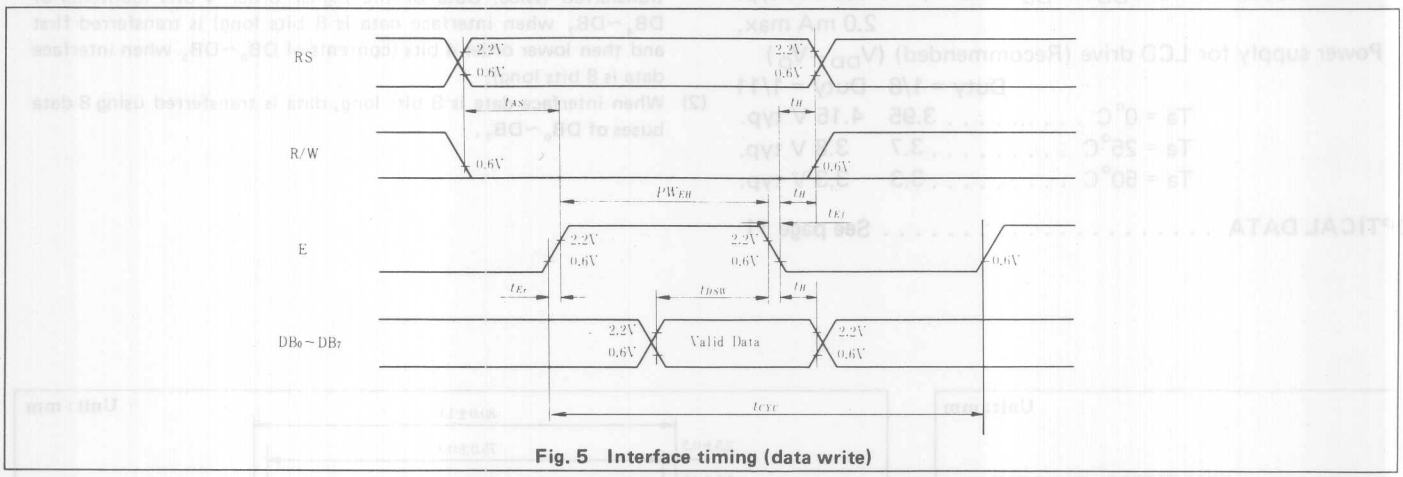


Fig. 5 Interface timing (data write)

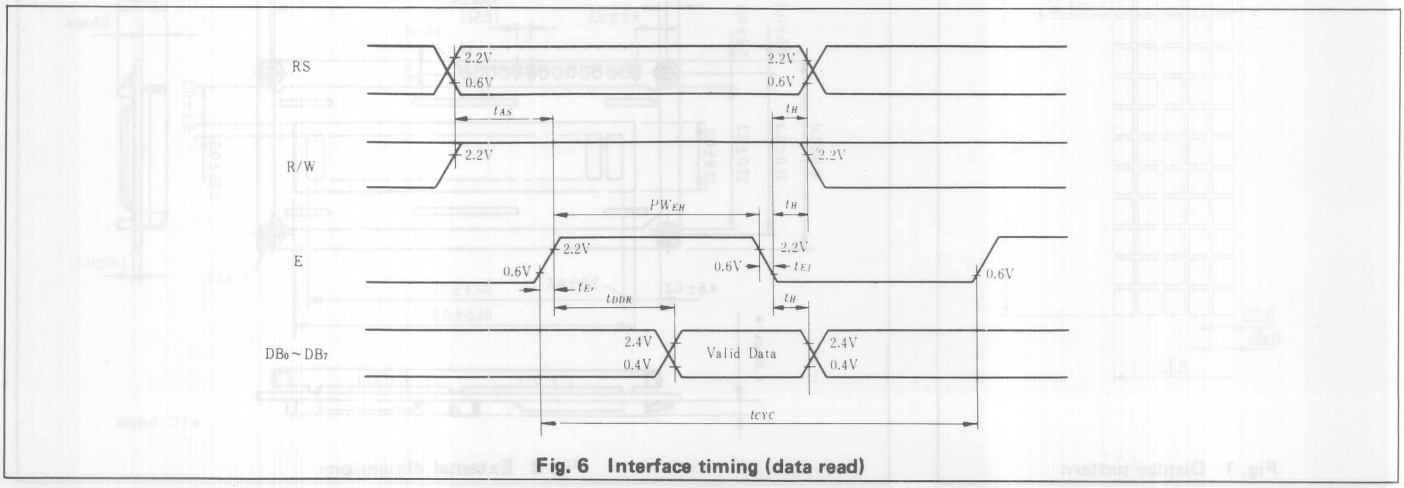


Fig. 6 Interface timing (data read)

LM015

- 16 character x 1 line
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	80W x 36H x 12D (max) mm
Effective display area	64.5W x 13.8H mm
Character size (5 x 7 dots)	3.15W x 5.5H mm
Character pitch	3.75 mm
Dot size	0.55W x 0.7H mm
Weight	about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.6 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	0.5 mA typ.
	2.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)	Duty = 1/8
Ta = 0°C	3.95 V typ.
Ta = 25°C	3.7 V typ.
Ta = 50°C	3.3 V typ.

OPTICAL DATA ..... See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	V_{SS}	—	0V — Power supply
2	V_{DD}	—	+5V — Power supply
3	V_O	—	— — Power supply
4	RS	H/L	L: Instruction code input H: Data input
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)
6	E	H, H→L	Enable signal
7	DB0	H/L	Data bus line Note (1), (2)
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of $DB_4 \sim DB_7$ and $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of $DB_0 \sim DB_3$ when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of $DB_0 \sim DB_7$.

Unit: mm

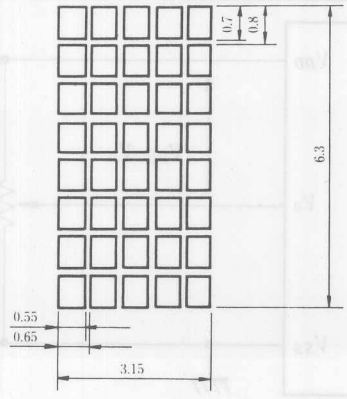


Fig. 1 Display pattern

Unit: mm

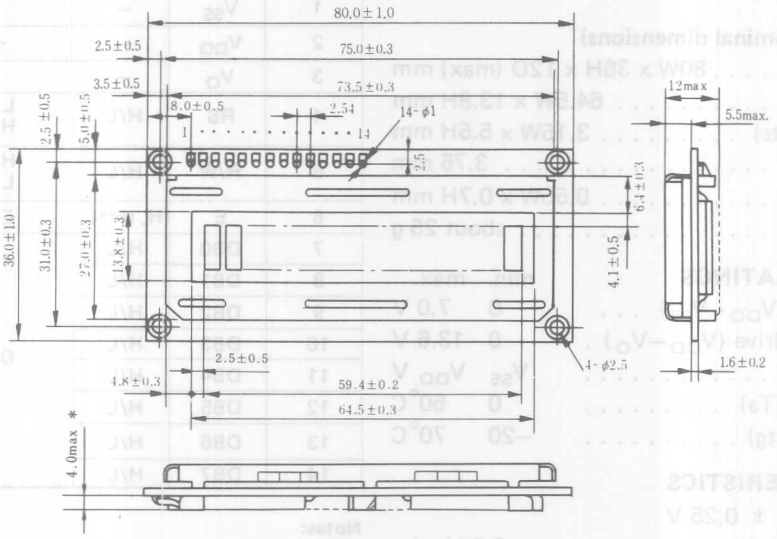


Fig. 2 External dimensions

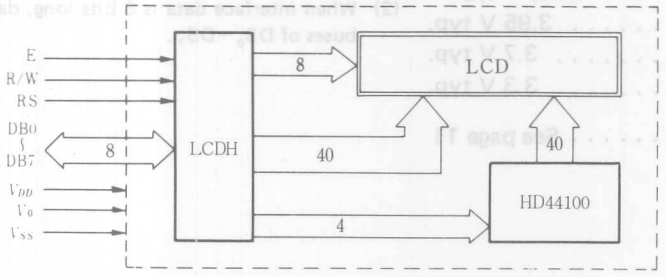
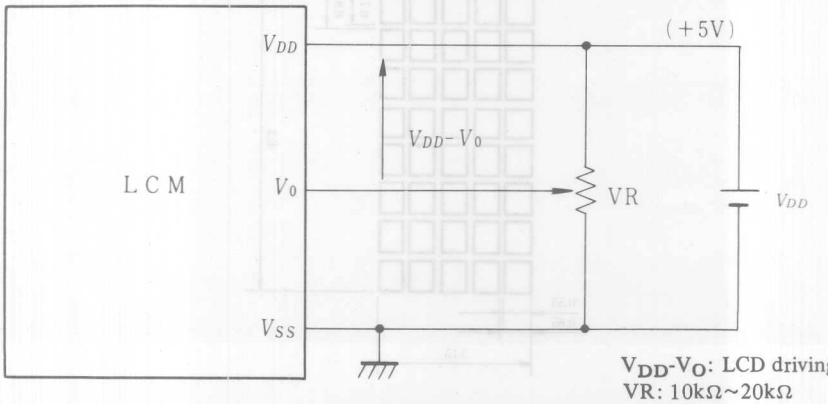


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

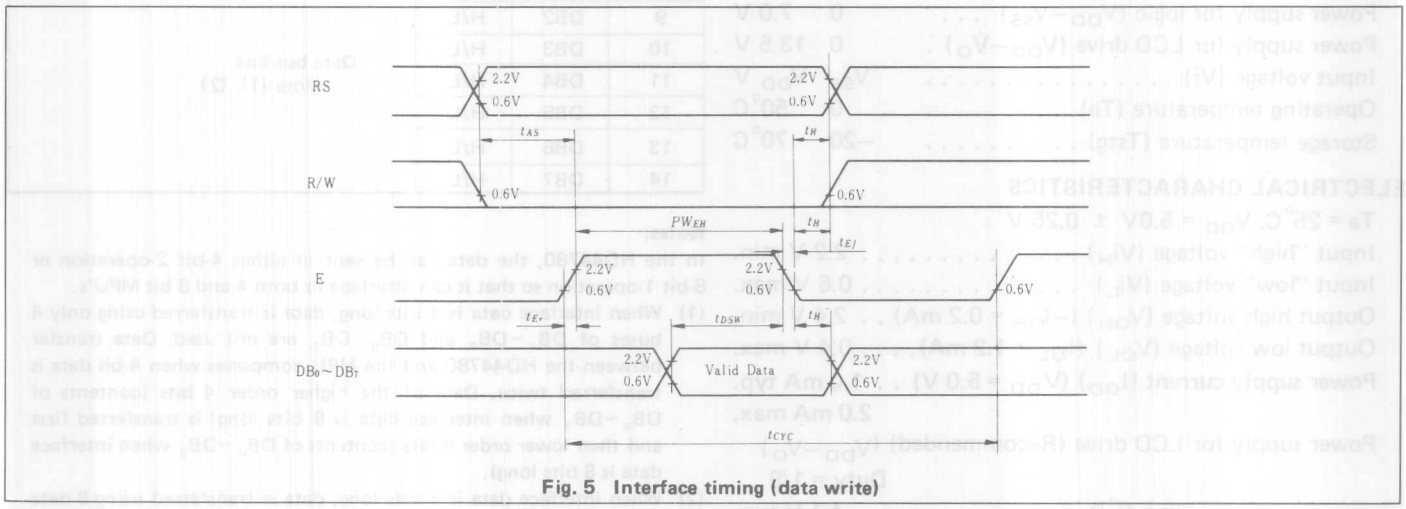


Fig. 5 Interface timing (data write)

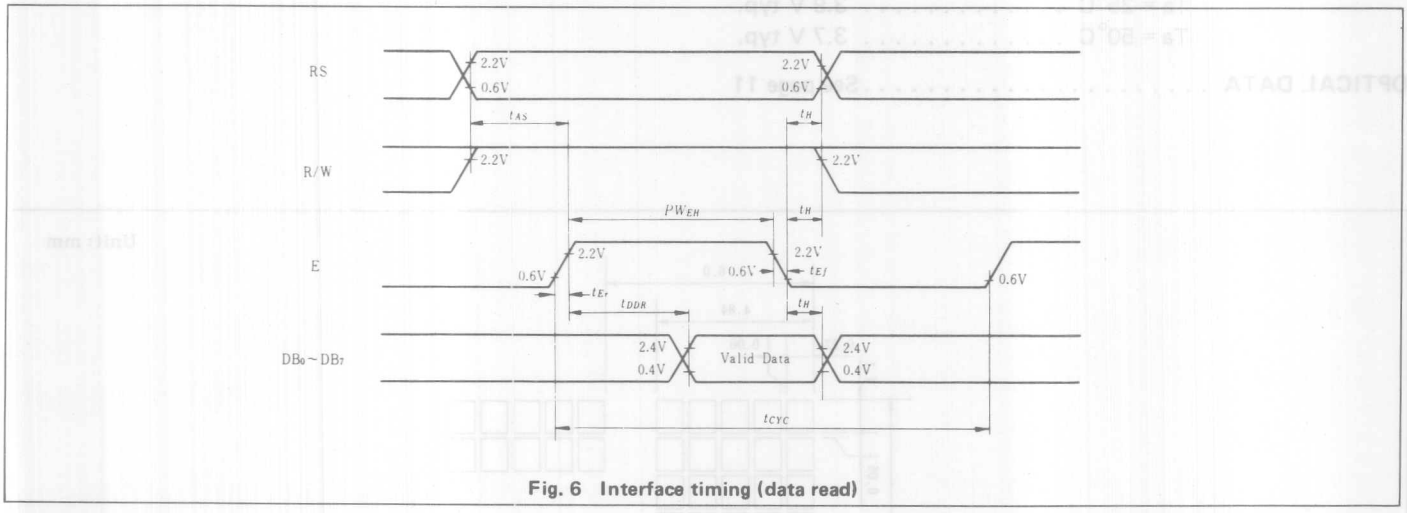


Fig. 6 Interface timing (data read)

LM568AF

- 16 character x 1 line
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 122W x 33H x 12.0T (max.) mm
Effective display area . . . . . 99W x 13H mm
Character size (5 x 7 dots) . . . . . 4.84W x 8.06H mm
Character pitch . . . . . 6.0 mm
Dot size . . . . . 0.92W x 1.1H mm
Weight . . . . . about 50 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$) . . .	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$) .	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0V ± 0.25 V
Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . . 2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
2.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/8
Ta = 0°C . . . . . 4.1 V typ.
Ta = 25°C . . . . . 3.9 V typ.
Ta = 50°C . . . . . 3.7 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.
(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).
(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

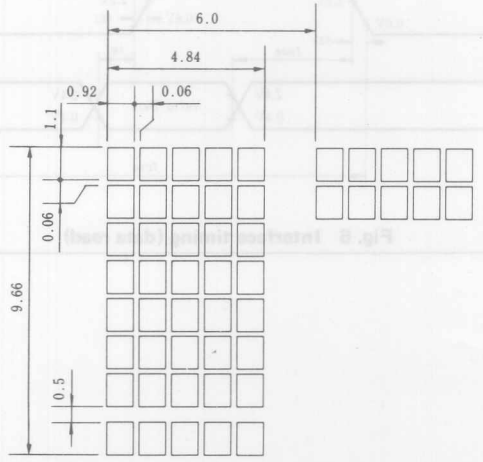


Fig. 1 Display pattern

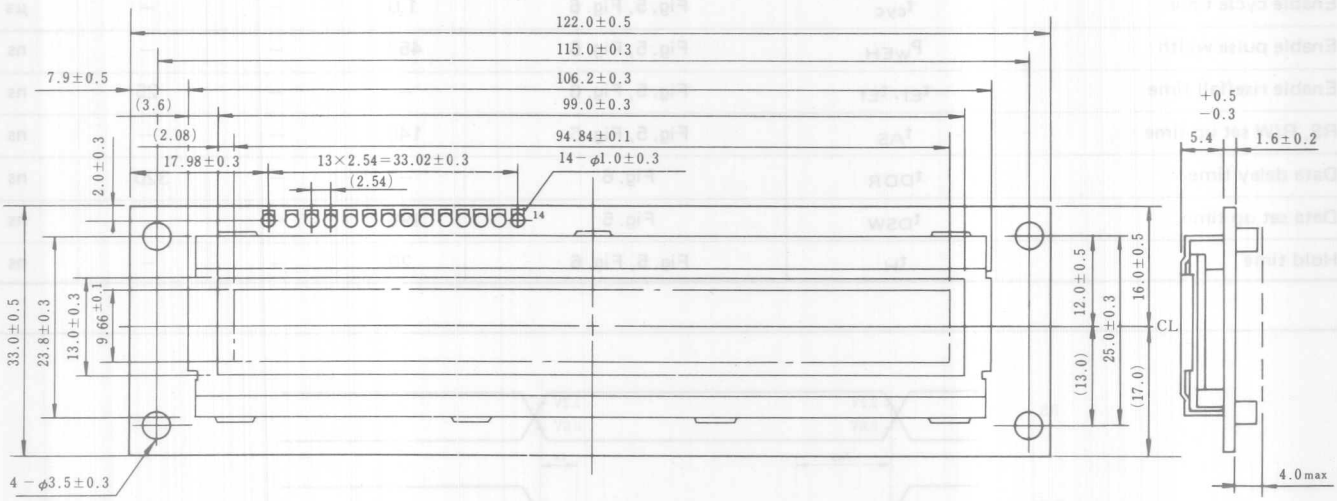


Fig. 2 External dimension

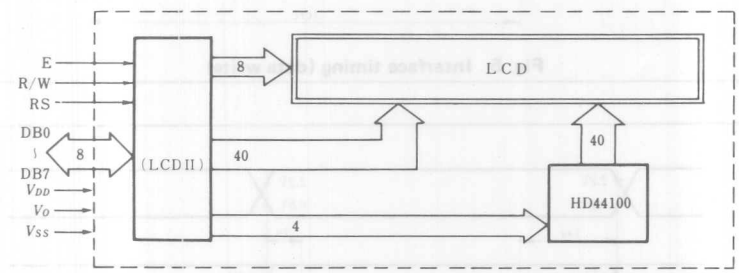
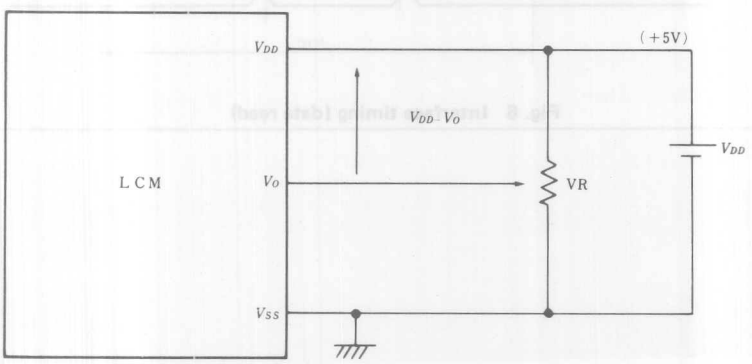


Fig. 3 Block diagram



$V_{DD} - V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

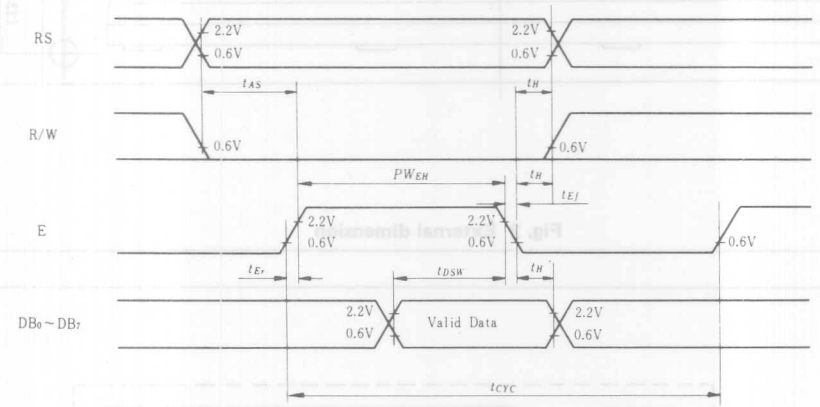


Fig. 5 Interface timing (data write)

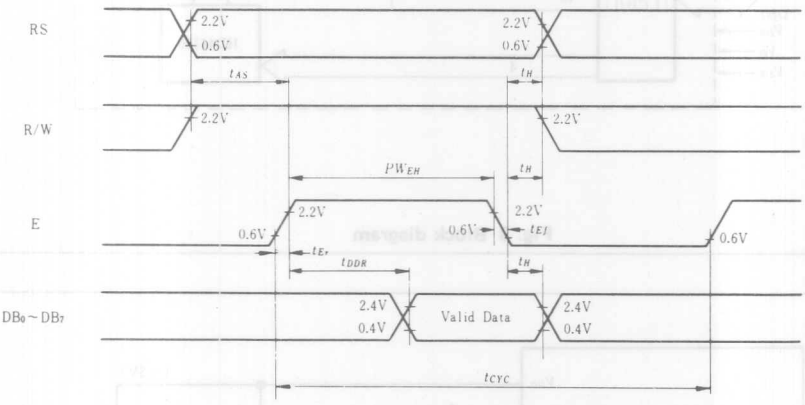


Fig. 6 Interface timing (data read)

LM020L

- 16 character x 1 line
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	80W x 36H x 12T (max.) mm
Effective display area	64.5W x 13.8H mm
Character size (5 x 7 dots)	3.07W x 5.73H mm
Characrer pitch	3.77 mm
Dot size	0.55W x 0.75H mm
Weight	about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

$Ta = 25°C$, $V_{DD} = 5.0\ V \pm 0.25\ V$

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH} = 0.2$ mA)	2.4 V min.
Output low voltage (V_{OL}) ($I_{OL} = 1.2$ mA)	0.4 V max.
Power supply current (I_{DD}) ($V_{DD} = 5.0$ V)	1.0 mA typ. 2.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$) Duty = 1/16	
Ta = 0°C	4.6 V typ.
Ta = 25°C	4.4 V typ.
Ta = 50°C	4.2 V typ.

OPTICAL DATA ..... See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	V_{SS}	—	0V (Power supply)
2	V_{DD}	—	+5V (Power supply)
3	V_O	—	— (Power supply)
4	RS	H/L	L: Instruction code input H: Data input
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)
6	E	H, H→L	Enable signal
7	DB0	H/L	Data bus line Note (1), (2)
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of $DB_4 \sim DB_7$ and $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of $DB_0 \sim DB_3$ when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of $DB_0 \sim DB_7$.

Unit: mm

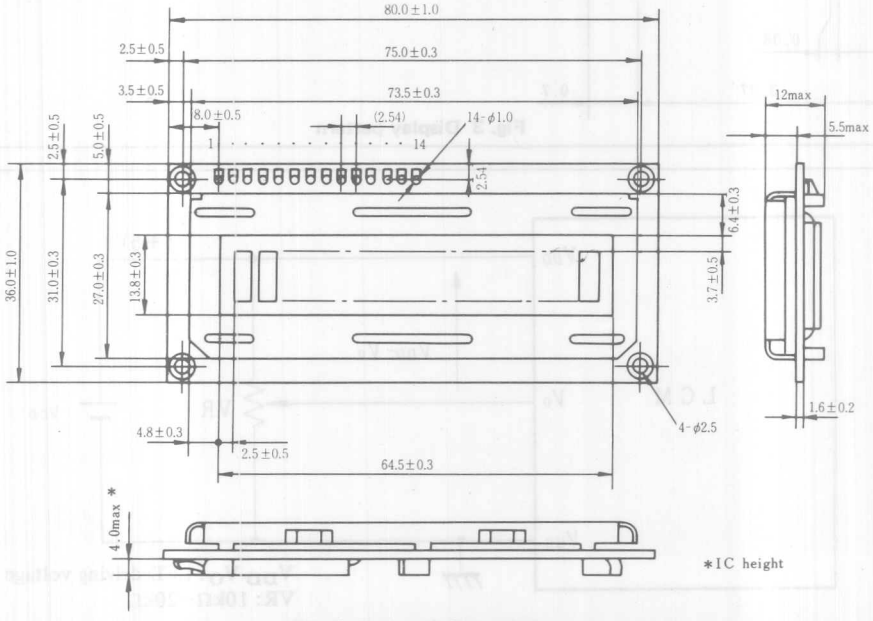


Fig. 1 External dimension

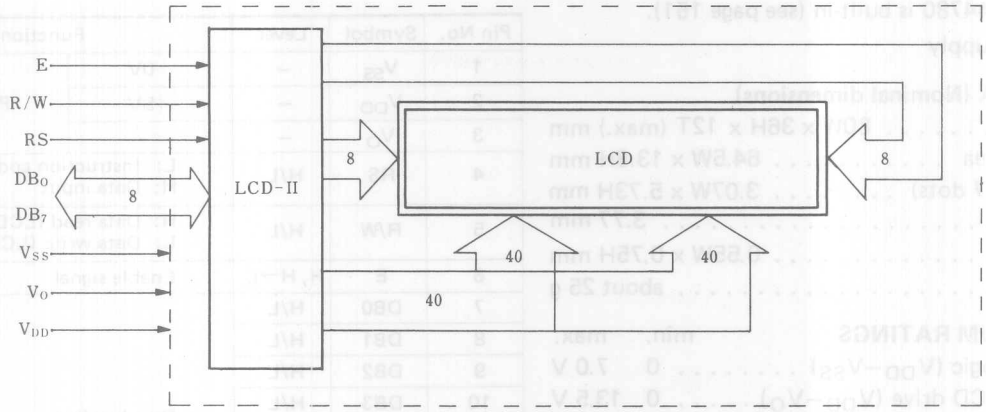


Fig. 2 Block diagram

Unit: mm

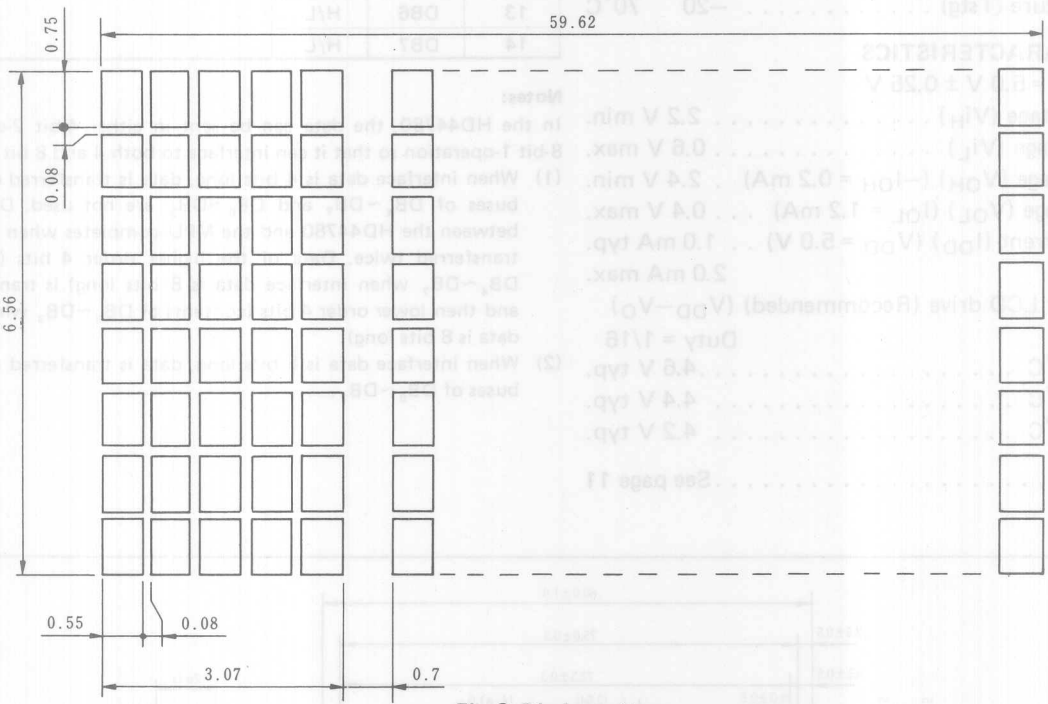


Fig. 3 Display pattern

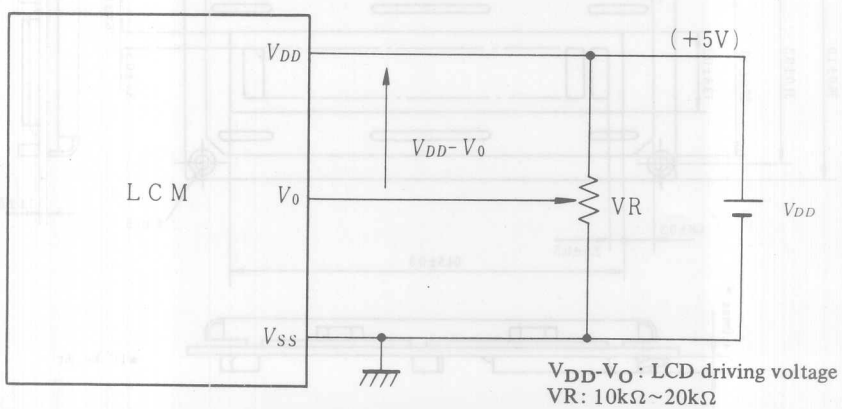


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

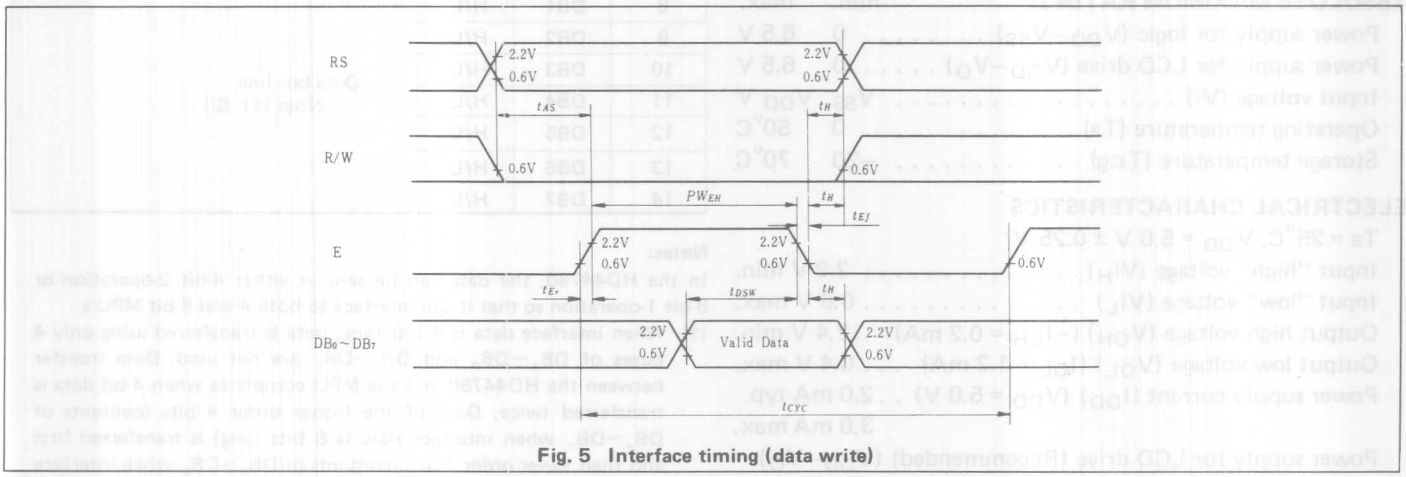


Fig. 5 Interface timing (data write)

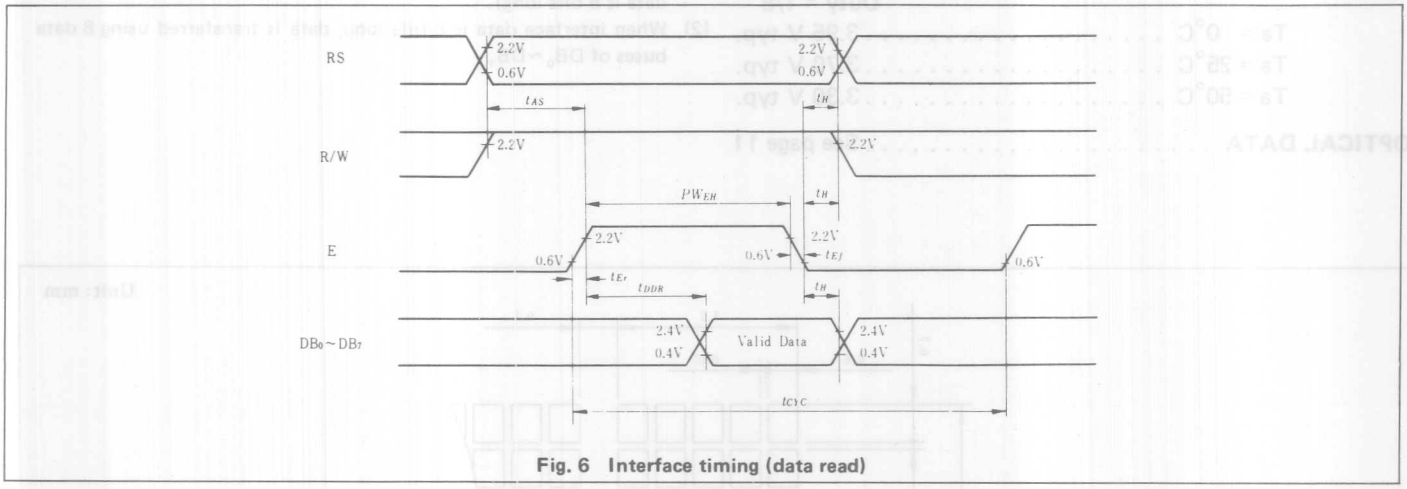


Fig. 6 Interface timing (data read)

LM070L

- 20 character x 1 line
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	105W x 39H x 11T (max.) mm
Effective display area	84W x 13.0H mm
Character size (5 x 7 dots)	3.2W x 5.2H mm
Character pitch	3.9 mm
Dot size	0.6W x 0.7H mm
Weight	about 50 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	6.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	2.0 mA typ.
	3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)	Duty = 1/8
Ta = 0°C	3.95 V typ.
Ta = 25°C	3.70 V typ.
Ta = 50°C	3.30 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	—	0V	Power supply
2	V_{DD}	—	+5V	
3	V_O	—	—	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of $DB_4 \sim DB_7$ and $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of $DB_0 \sim DB_3$ when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of $DB_0 \sim DB_7$.

Unit: mm

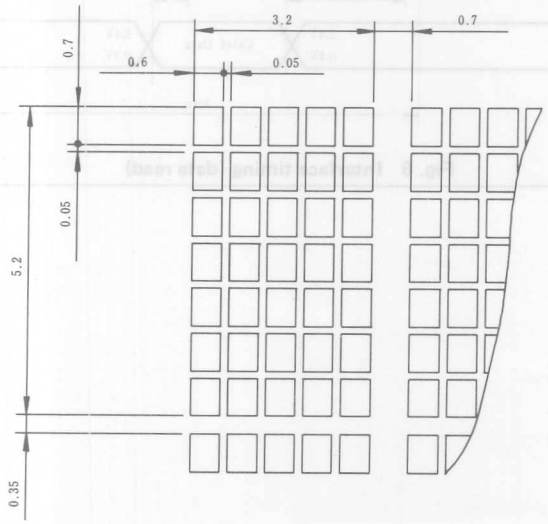


Fig. 1 Display pattern

HITACHI

Unit: mm

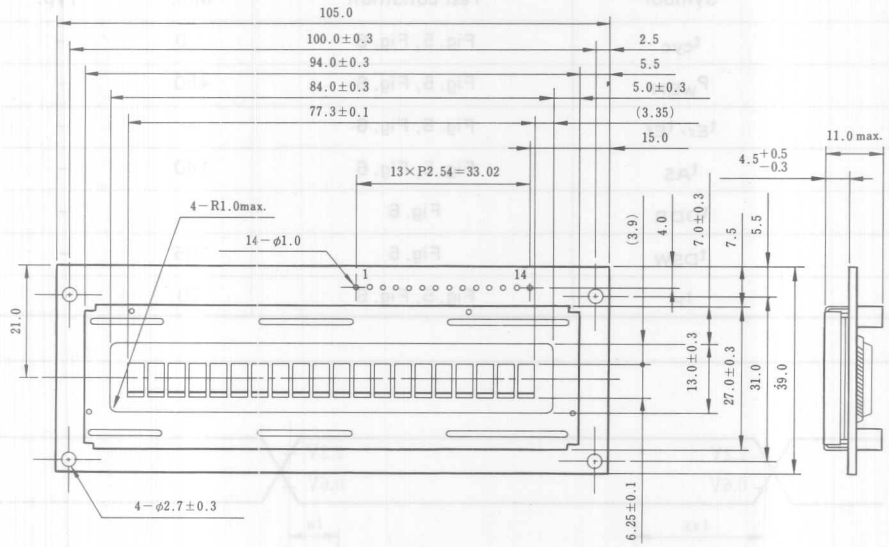
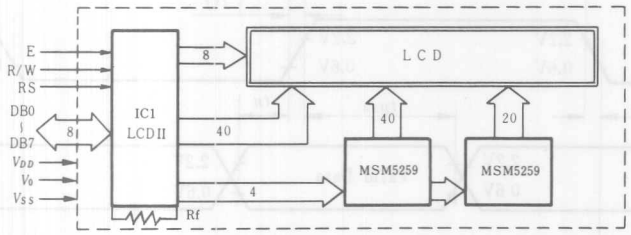
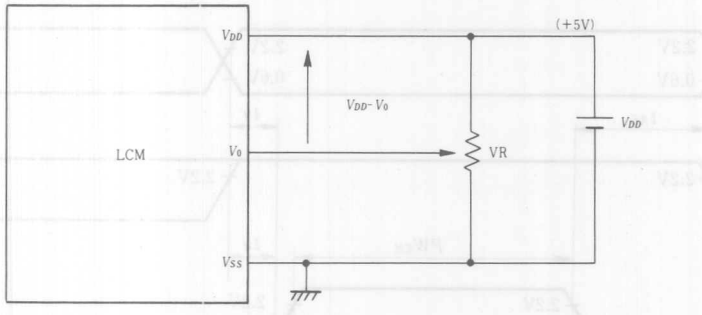


Fig. 2 External dimension



Rf=91kΩ

Fig. 3 Block diagram



$V_{DD} - V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

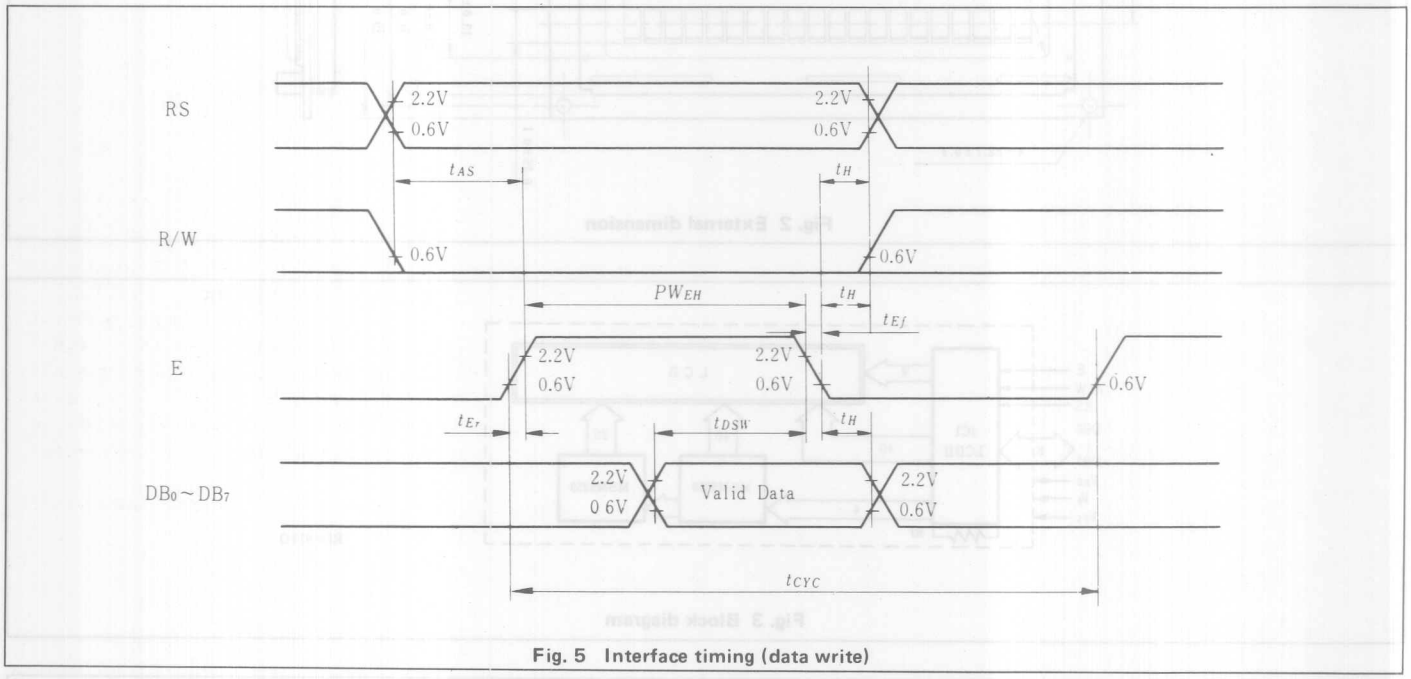


Fig. 5 Interface timing (data write)

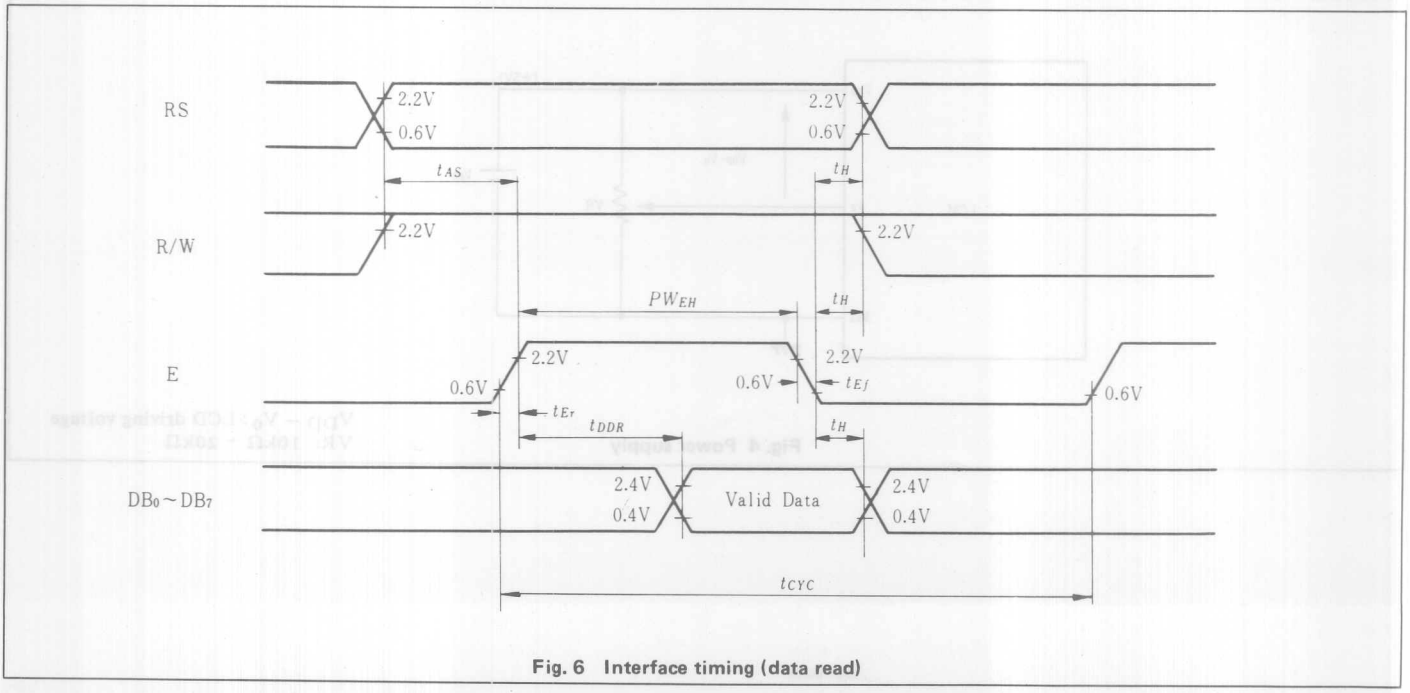


Fig. 6 Interface timing (data read)

LM038

- 20 character x 1 line
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 182W x 35.5H(max.) x 13D (max.) mm
Effective display area . . . . . 154.0W x 15.3H mm
Character size (5 x 7 dots) . . . . . 6.7W x 9.4H mm
Character pitch . . . . . 7.4 mm
Dot size . . . . . 1.3W x 1.3H mm
Weight . . . . . about 65 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . 2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 2.0 mA typ.
5.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/8
Ta = 0°C . . . . . 4.1 V typ.
Ta = 25°C . . . . . 3.7 V typ.
Ta = 50°C . . . . . 3.1 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	—	0V	Power supply
2	V_{DD}	—	+5V	
3	V_O	—	—	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4 ~ DB_7 and DB_0 ~ DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4 ~ DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0 ~ DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0 ~ DB_7.

Unit: mm

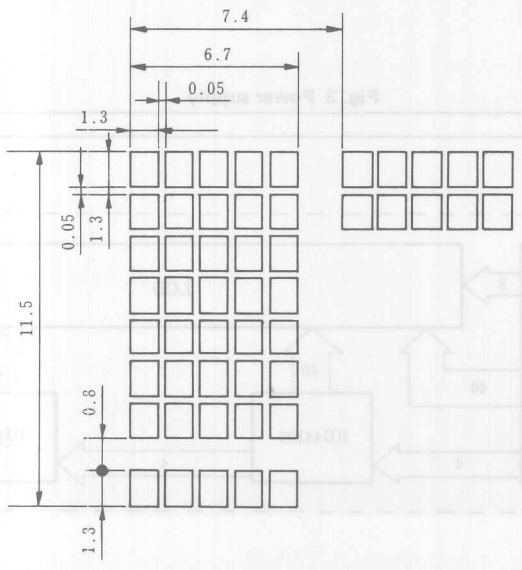


Fig. 1 Display pattern

Unit: mm

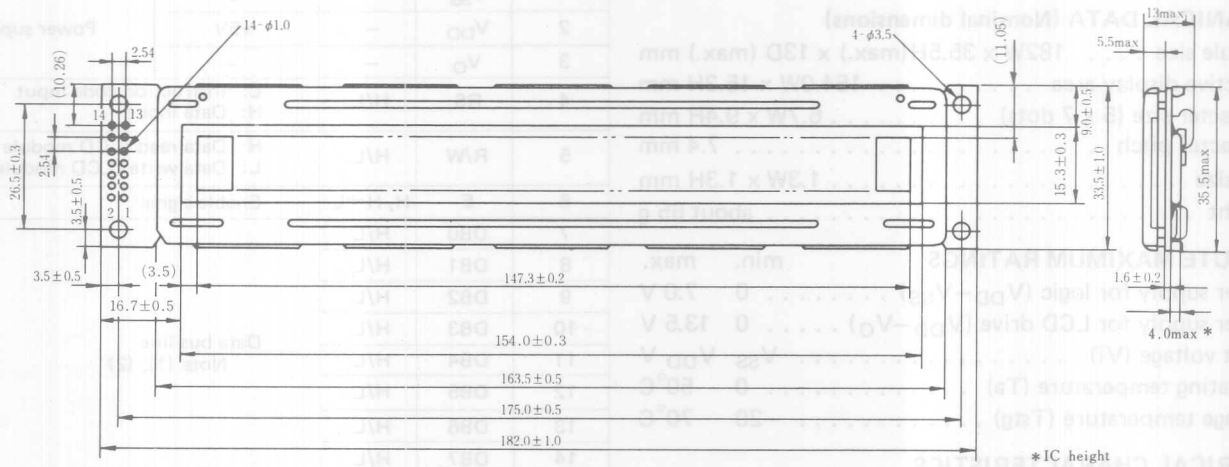
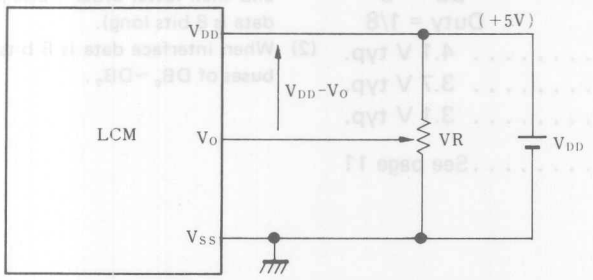


Fig. 2 External dimension



V_{DD}-V_O: LCD driving voltage
VR: 10 kΩ ~ 20 kΩ

Fig. 3 Power supply

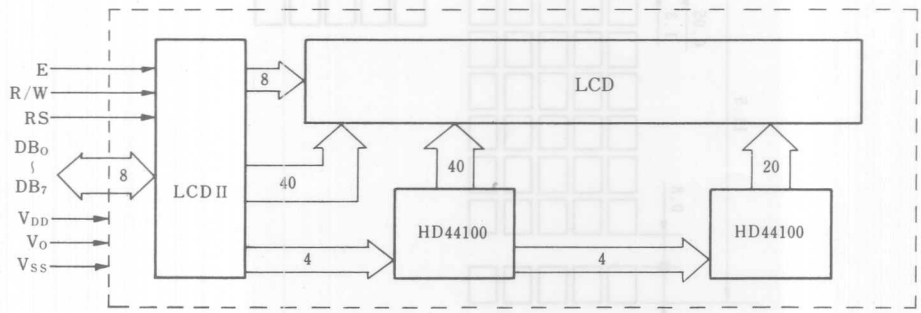


Fig. 4 Block diagram

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

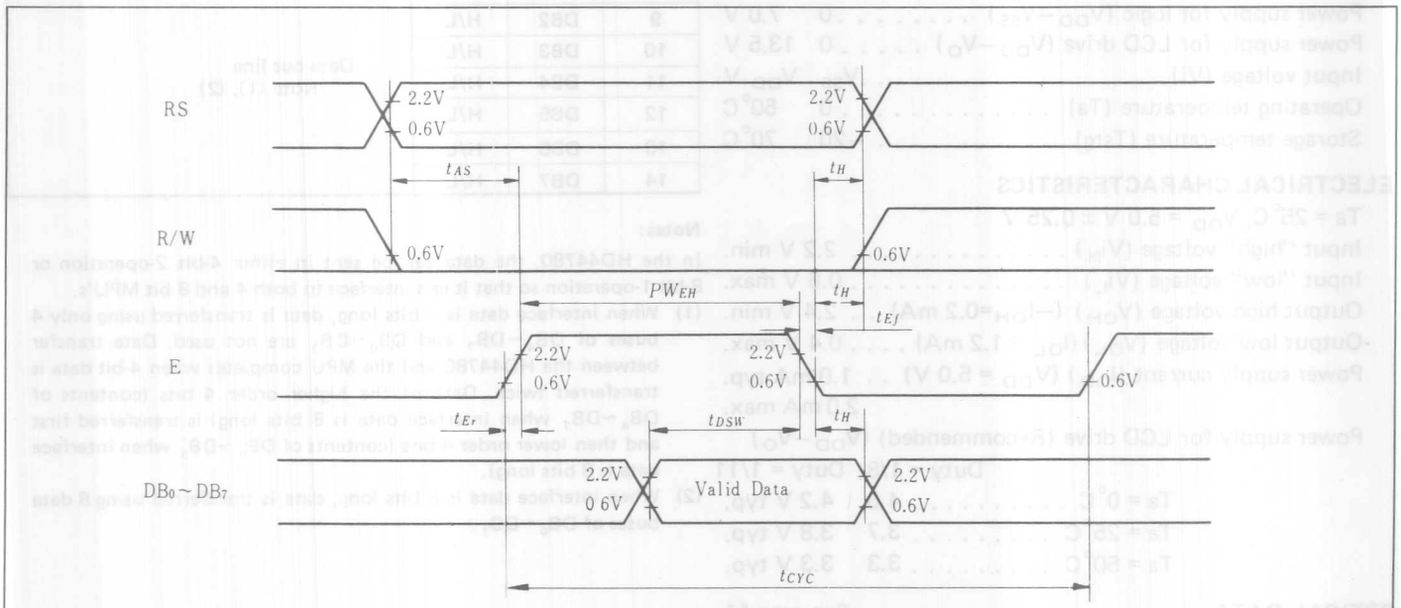


Fig. 5 Interface timing (data write)

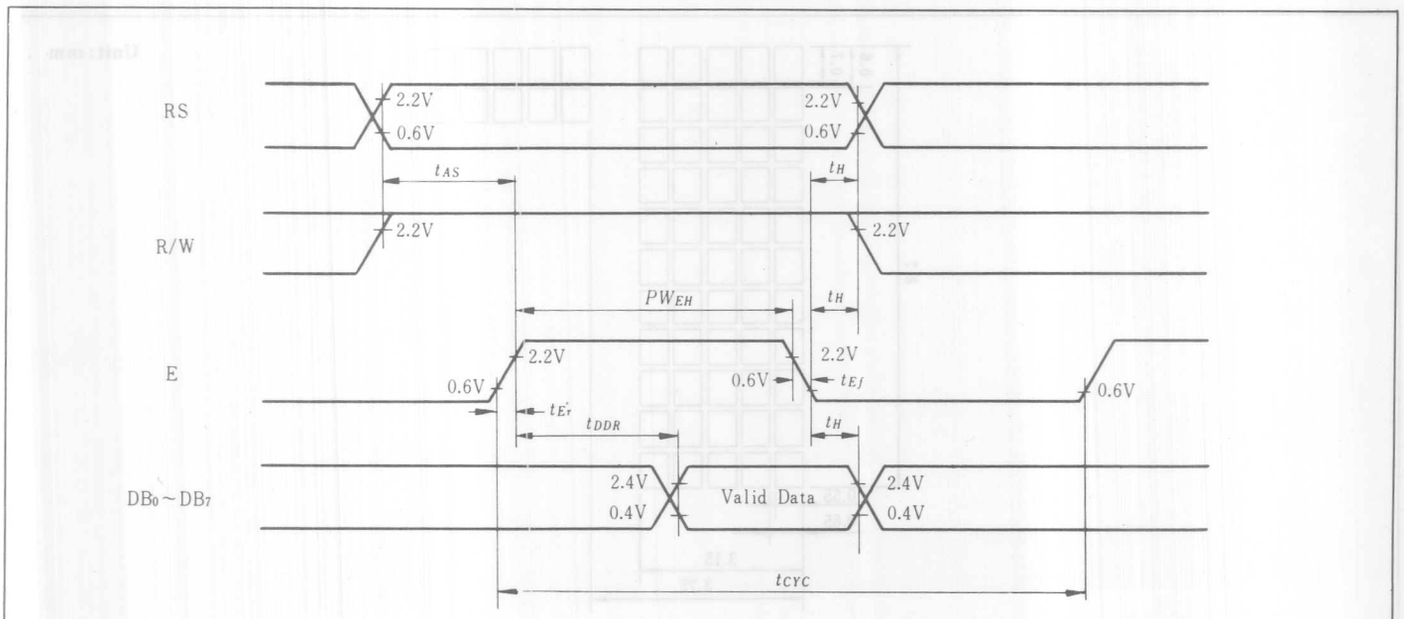


Fig. 6 Interface timing (data read)

LM027

- 24 character x 1 line
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	126W x 36H x 12T (max.) mm
Effective display area	100W x 13.8H mm
Character size (5 x 10 dots)	3.15W x 7.9H mm
Character pitch	3.75 mm
Dot size	0.55W x 0.7H mm
Weight	about 40 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.	
Input "low" voltage (Vi_L)	0.6 V max.	
Output high voltage (V_{OH}) ($-I_{OH}$=0.2 mA)	2.4 V min.	
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.	
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ.	2.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

	Duty = 1/8	Duty = 1/11
Ta = 0°C	4.0	4.2 V typ.
Ta = 25°C	3.7	3.8 V typ.
Ta = 50°C	3.3	3.3 V typ.

OPTICAL DATA See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	V_{SS}	—	0V (Power supply)
2	V_{DD}	—	+5V (Power supply)
3	V_O	—	— (Power supply)
4	RS	H/L	L: Instruction code input H: Data input
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)
6	E	H, H→L	Enable signal
7	DB0	H/L	Data bus line Note (1), (2)
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

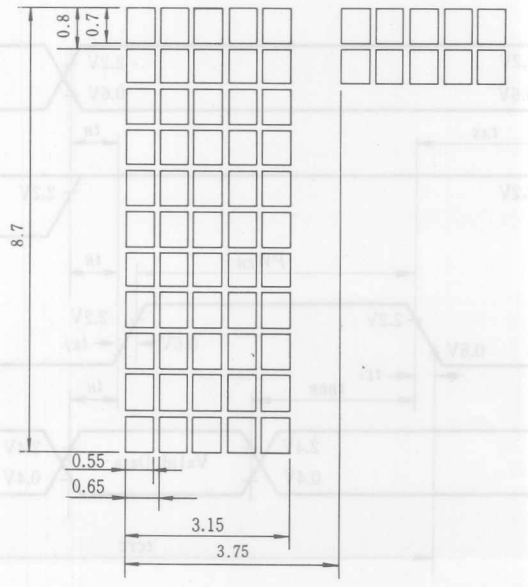


Fig. 1 Display pattern

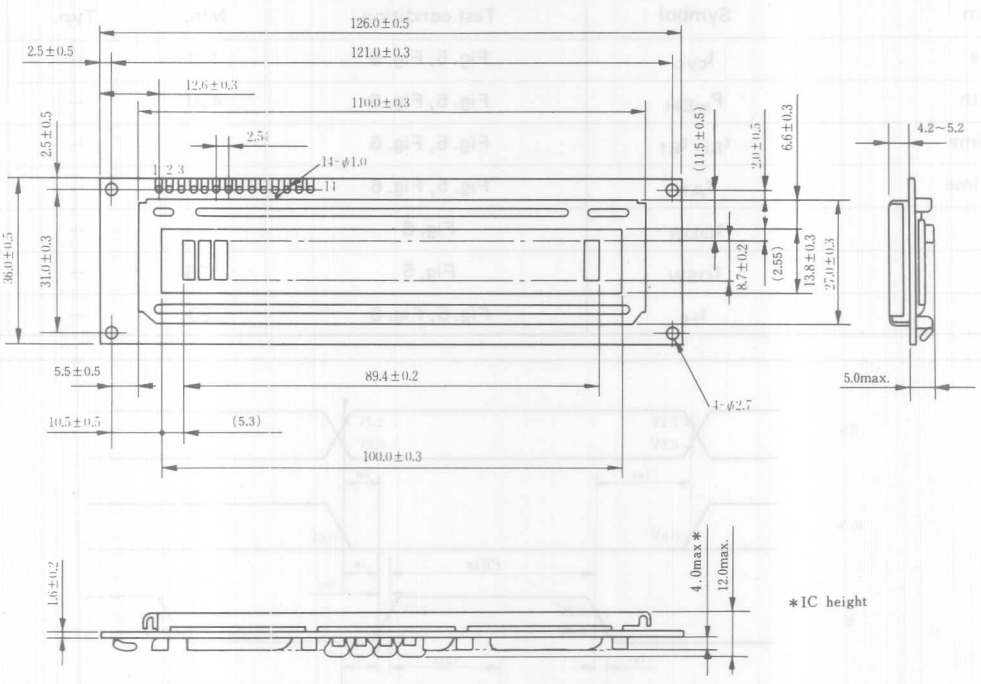


Fig. 2 External dimensions

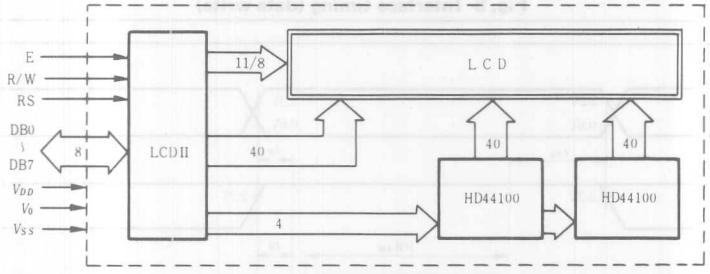


Fig. 3 Block diagram

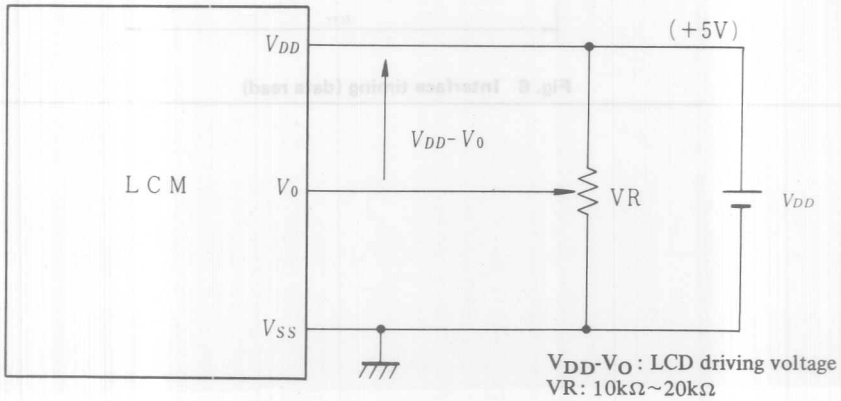


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

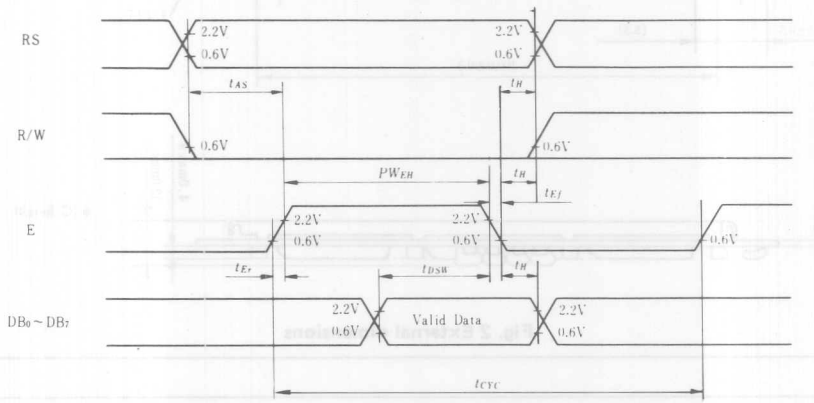


Fig. 5 Interface timing (data write)

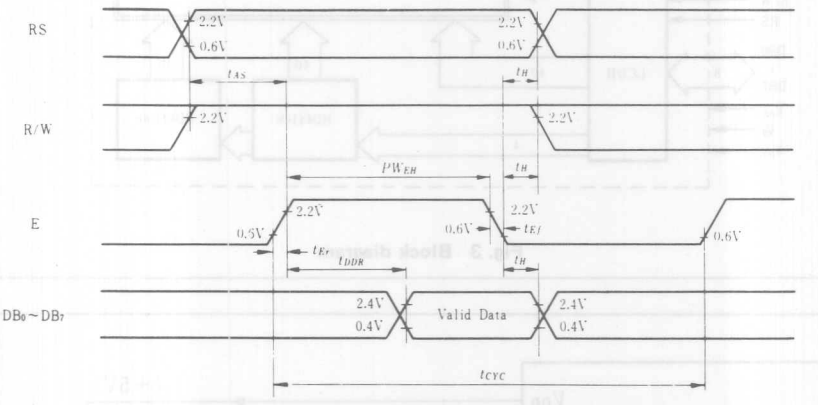


Fig. 6 Interface timing (data read)

H2571

- 32 character x 1 line
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . 174.5W x 33.0H (max.) x 13.4T (max.) mm
Effective display are . . . . . 132.5W x 14.0H mm
Character size (5 x 10 dots) . . . . . 3.15W x 7.9H mm
Character pitch . . . . . 3.85 mm
Dot size . . . . . 0.55W x 0.7H mm
Weight . . . . . about 60 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$) . . .	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2mA) . . 2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
2.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

	Duty = 1/8	Duty = 1/11
Ta = 0°C	3.95	4.15V typ.
Ta = 25°C	3.7	3.8V typ.
Ta = 50°C	3.3	3.3V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4 ~ DB_7 and DB_0 ~ DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4 ~ DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0 ~ DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0 ~ DB_7.

Unit: mm

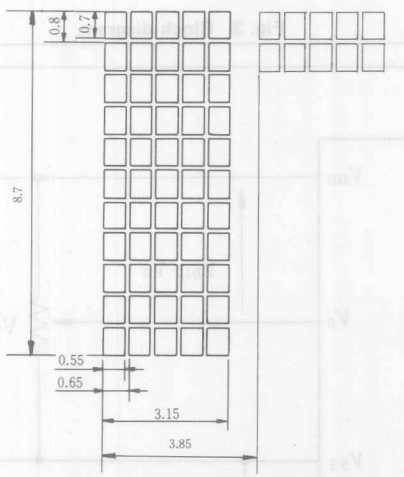


Fig. 1 Display pattern

Unit: mm

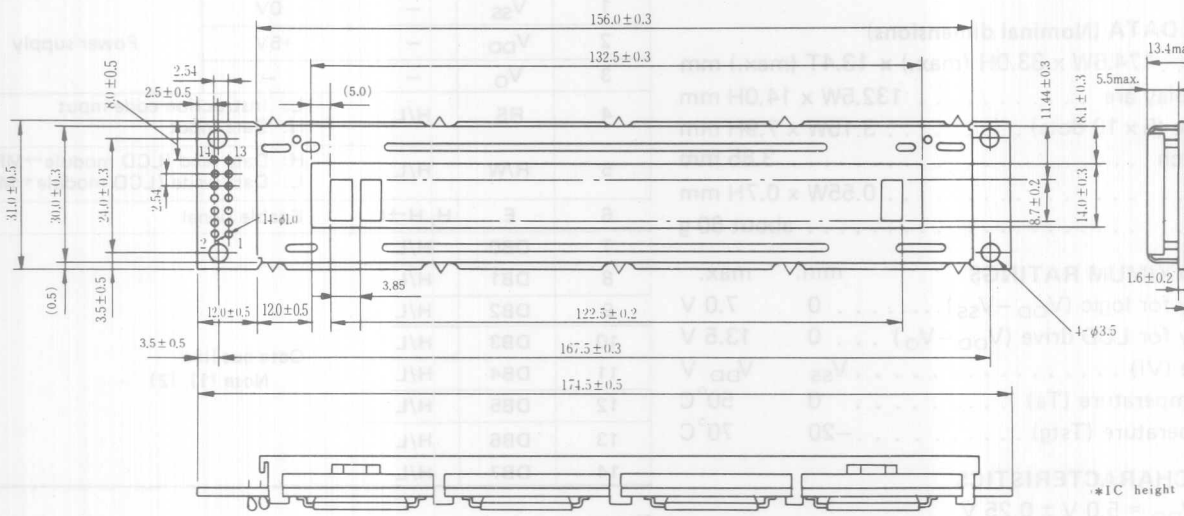


Fig. 2 External dimensions

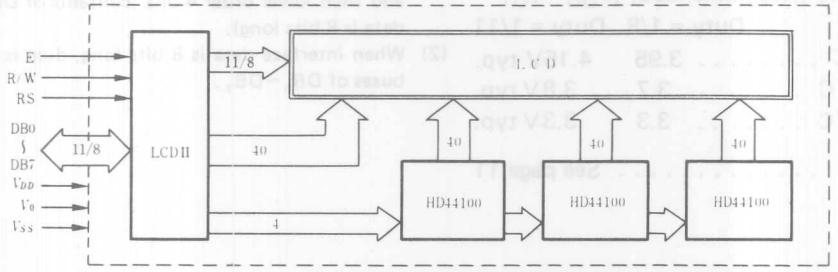
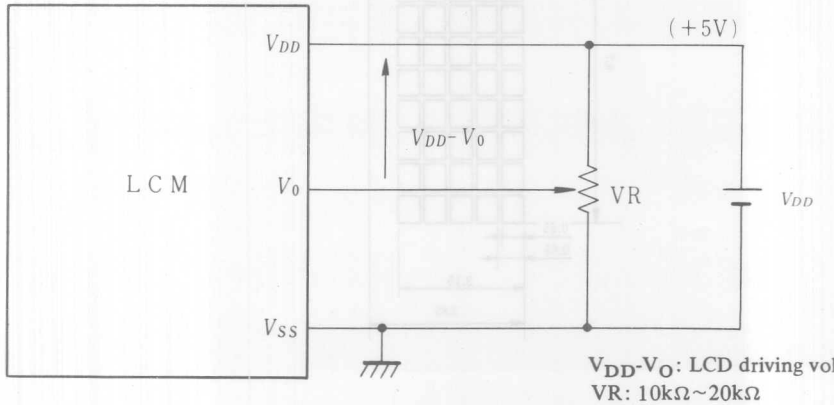


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

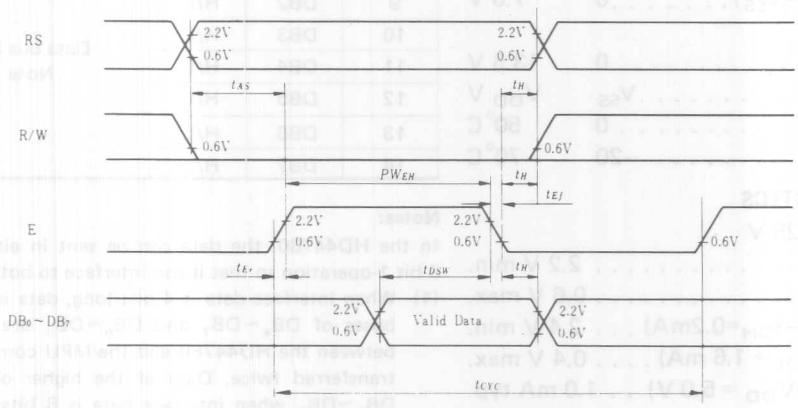


Fig. 5 Interface timing (data write)

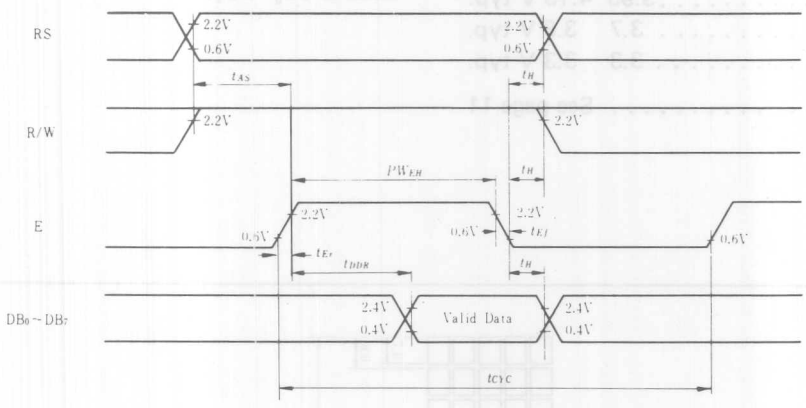


Fig. 6 Interface timing (data read)

H2572

- 40 character x 1 line
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . 182W x 35.5H (max.) x 13T (max.) mm
Effective display area . . . . . 154.0W x 15.3H mm
Character size (5 x 10 dots) . . . . . 3.15W x 7.9H mm
Character pitch . . . . . 3.75 mm
Dot size . . . . . 0.55W x 0.7H mm
Weight . . . . . about 65 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$=0.2mA) . . . 2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL}= 1.6 mA) . . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
2.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

	Duty = 1/8	Duty = 1/11
Ta = 0°C	3.95	4.15 V typ.
Ta = 25°C	3.7	3.8 V typ.
Ta = 50°C	3.3	3.3 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	—	0V	Power supply
2	V_{DD}	—	+5V	
3	V_O	—	—	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

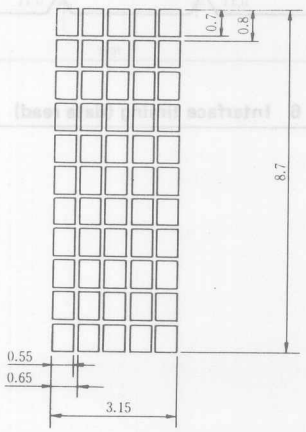


Fig. 1 Display pattern

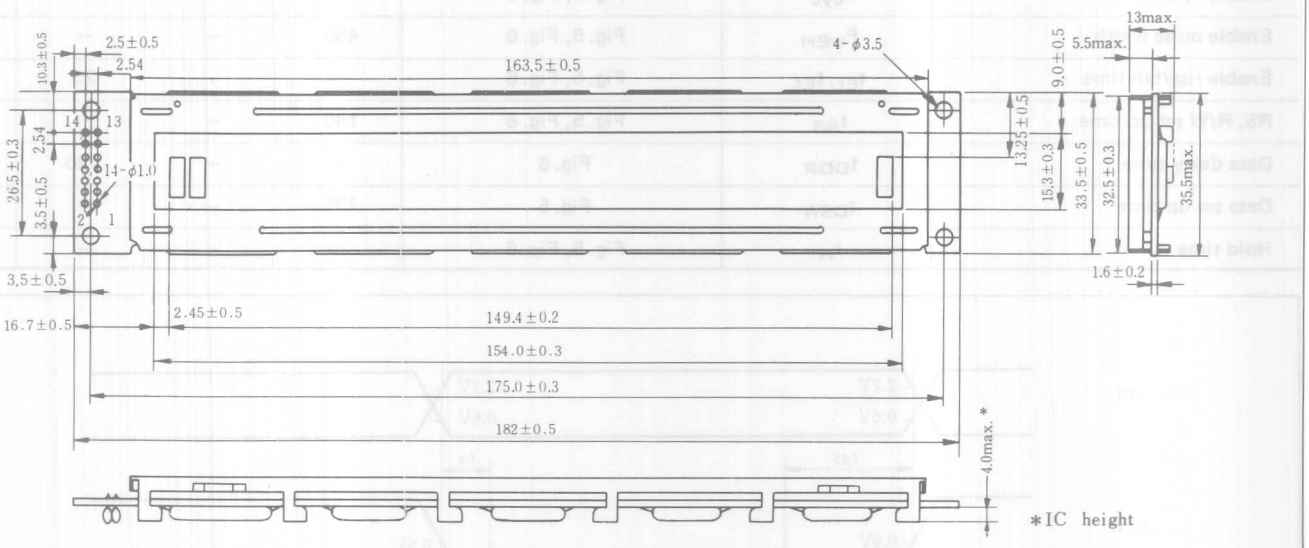


Fig. 2 External dimensions

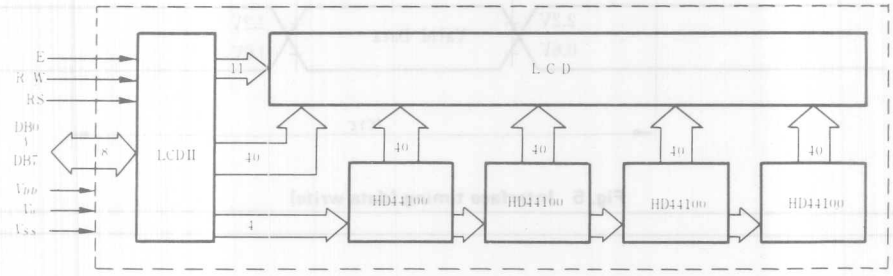


Fig. 3 Block diagram

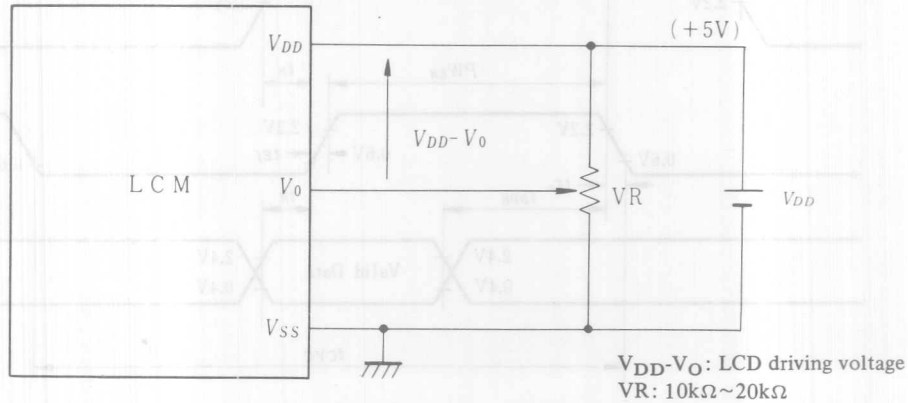


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

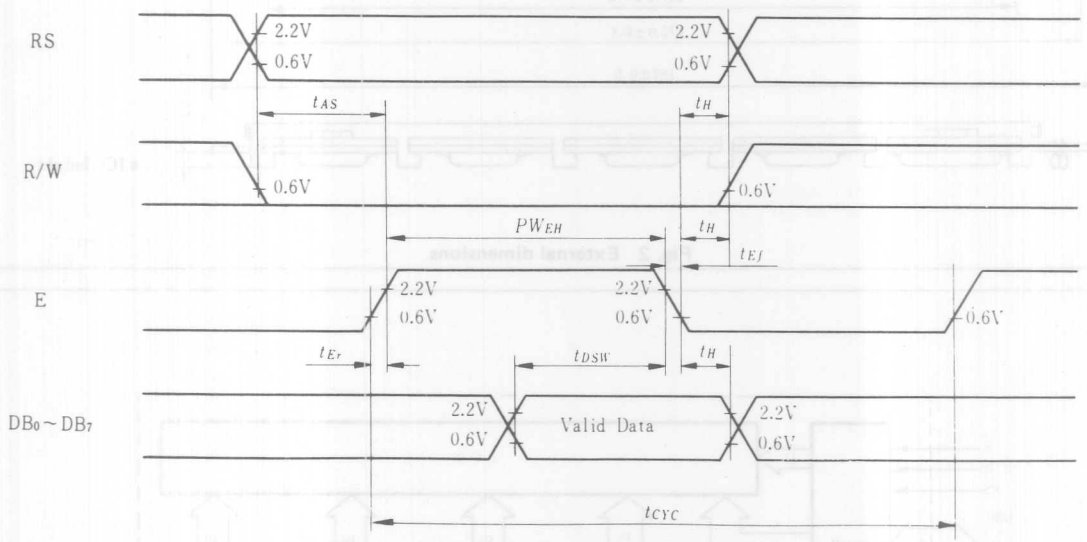


Fig. 5 Interface timing (data write)

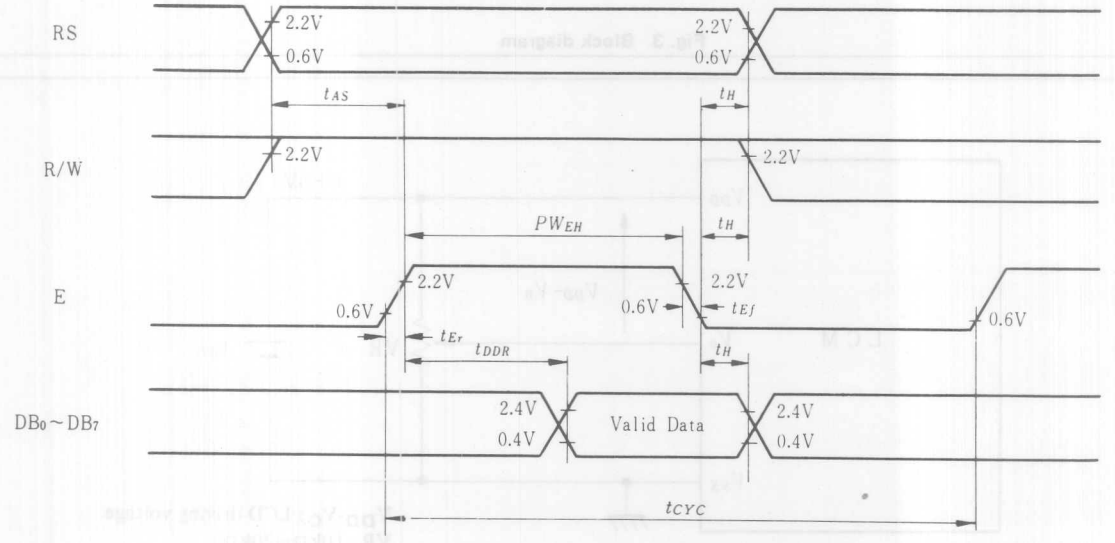


Fig. 6 Interface timing (data read)

LM058

- 40 character x 1 line
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	290W x 60H x 13.0T (max.) mm
Effective display area	245W x 19.0H mm
Character size (5 x 7 dots)	4.82W x 8.18H mm
Character pitch	5.82 mm
Dot size	0.9W x 1.1H mm
Weight	about 150 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$=0.2mA)	2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	0.5 mA typ. 2.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

Duty = 1/8

Ta = 0°C	4.3 V typ.
Ta = 25°C	3.9 V typ.
Ta = 50°C	3.3 V typ.

OPTICAL DATA ..... See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

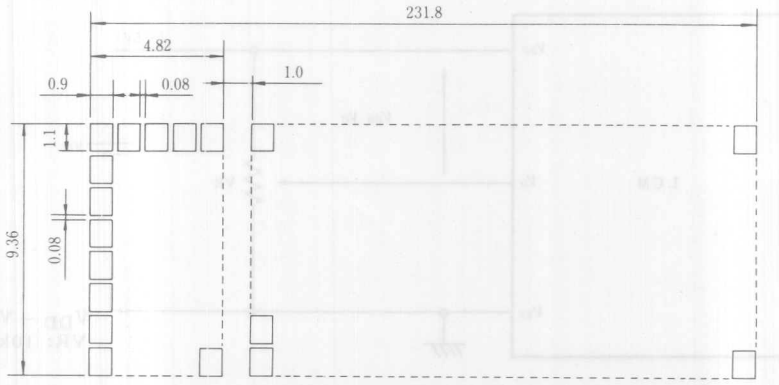


Fig. 1 Display pattern

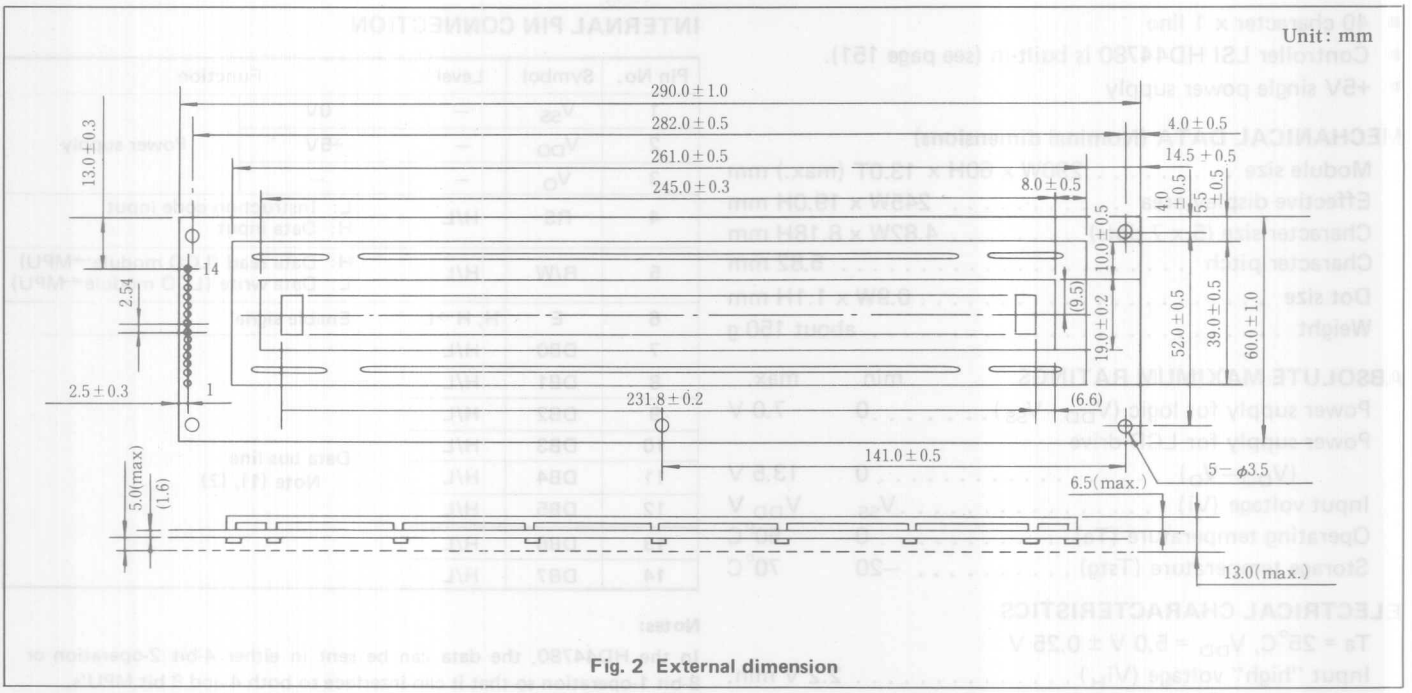


Fig. 2 External dimension

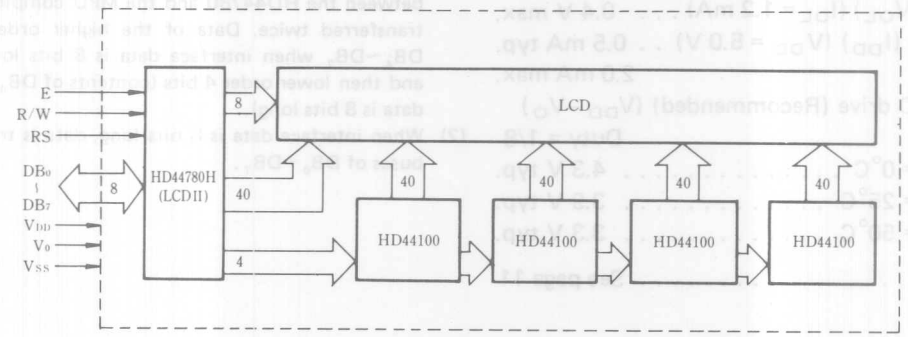
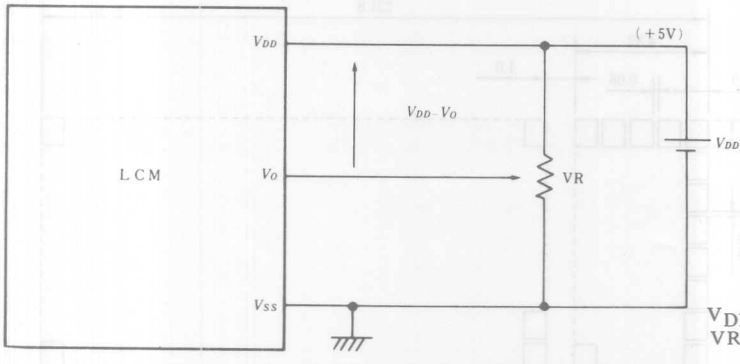


Fig. 3 Block diagram



$V_{DD} - V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

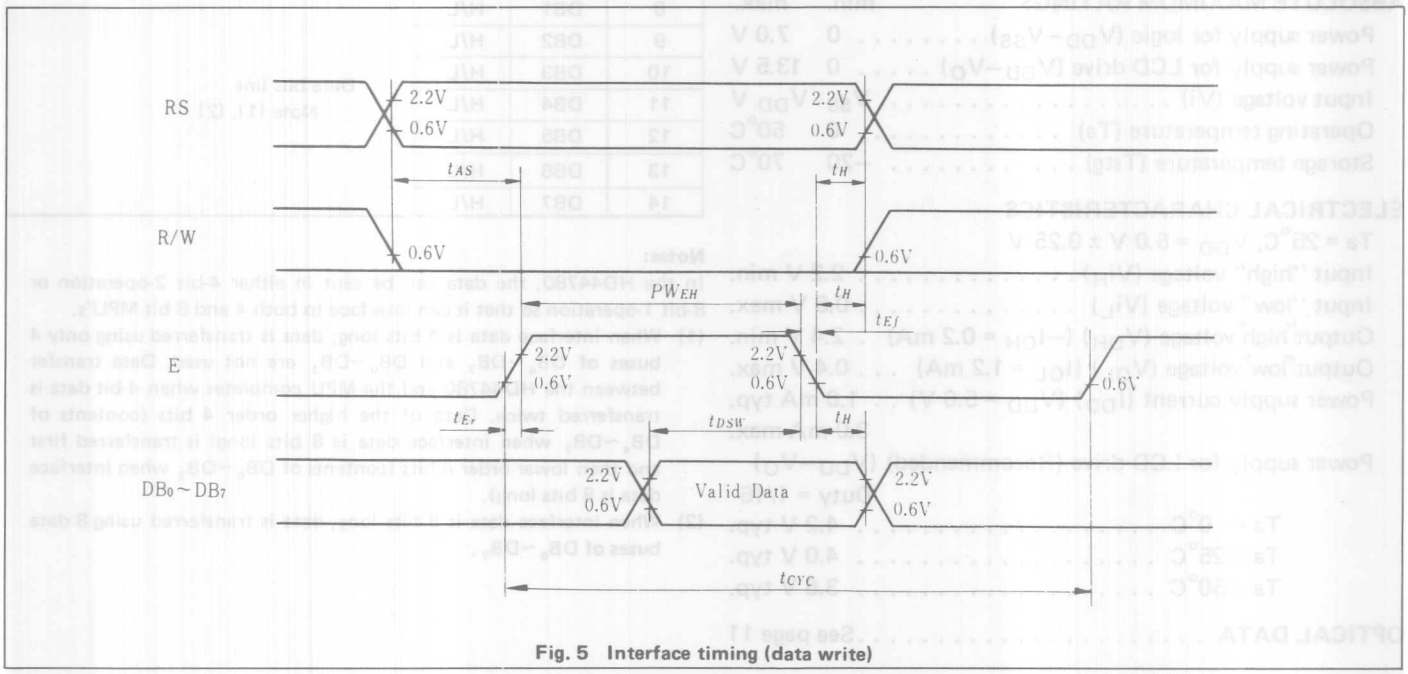


Fig. 5 Interface timing (data write)

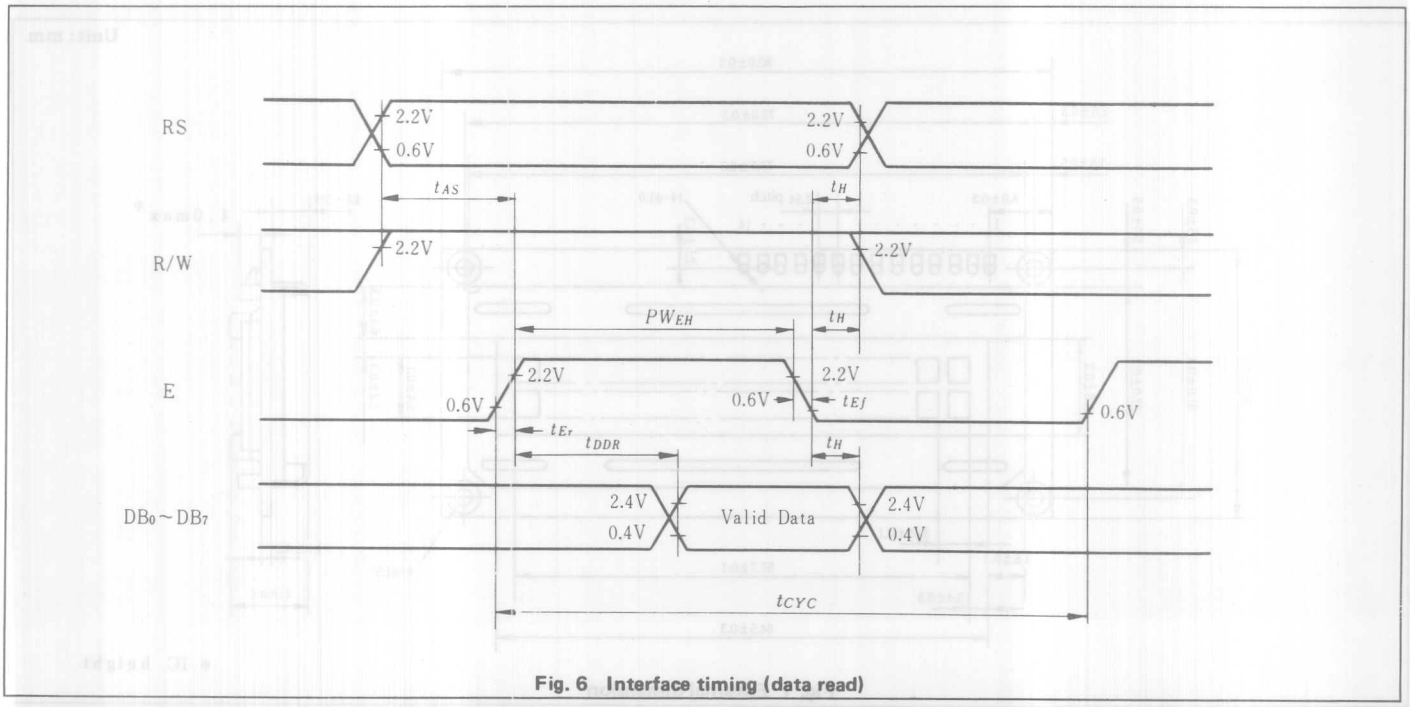


Fig. 6 Interface timing (data read)

LM052L

- 16 character x 2 lines
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	80W x 36H x 11T (max.) mm
Effective display area	64.5W x 13.8H mm
Character size (5 x 7 dots)	2.95W x 3.8H mm
Character pitch	3.65 mm
Dot size	0.55W x 0.5H mm
Weight	about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ.
	3.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

Duty = 1/16

Ta = 0°C	4.2 V typ.
Ta = 25°C	4.0 V typ.
Ta = 50°C	3.6 V typ.

OPTICAL DATA ..... See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

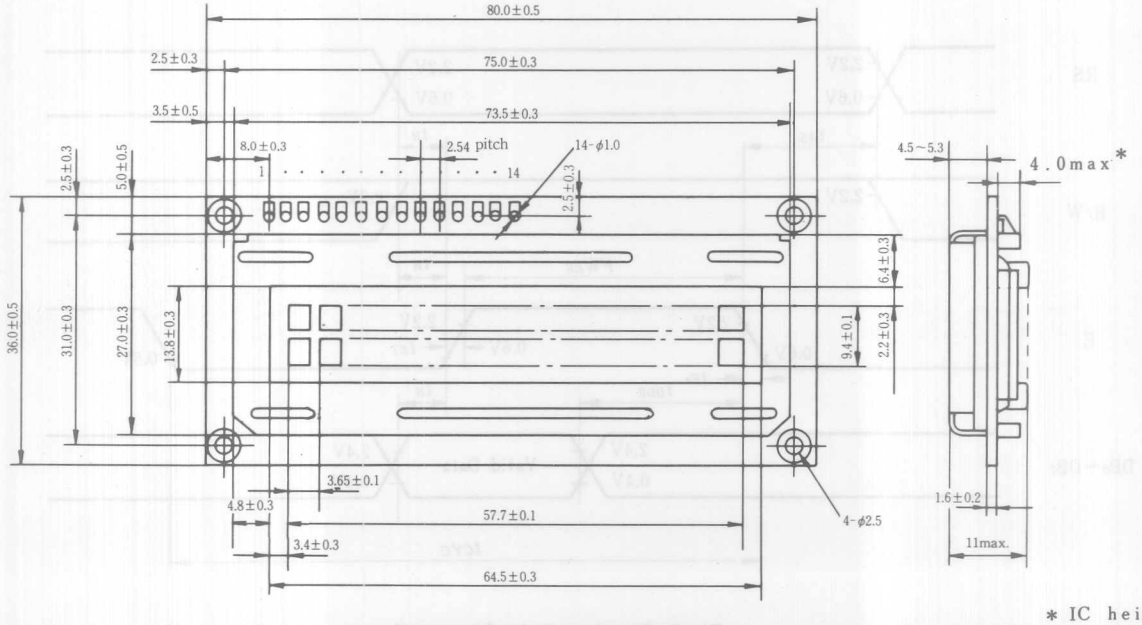


Fig. 1 External dimension

Unit: mm

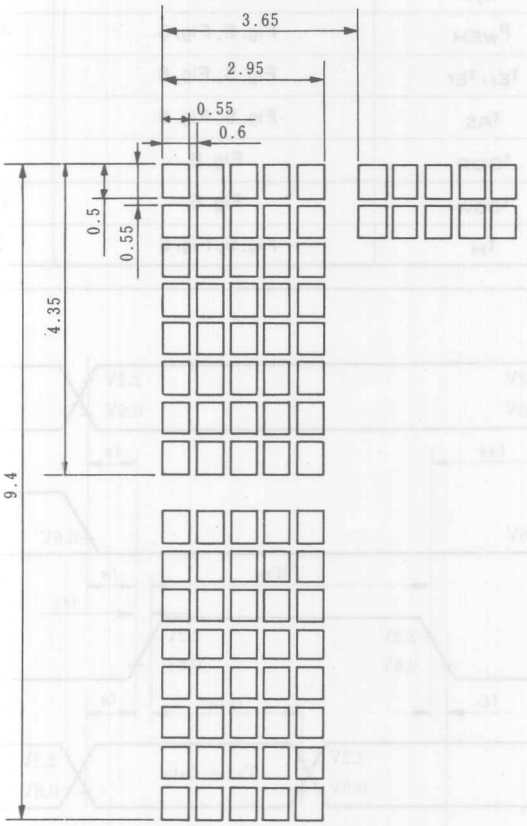


Fig. 2 Display pattern

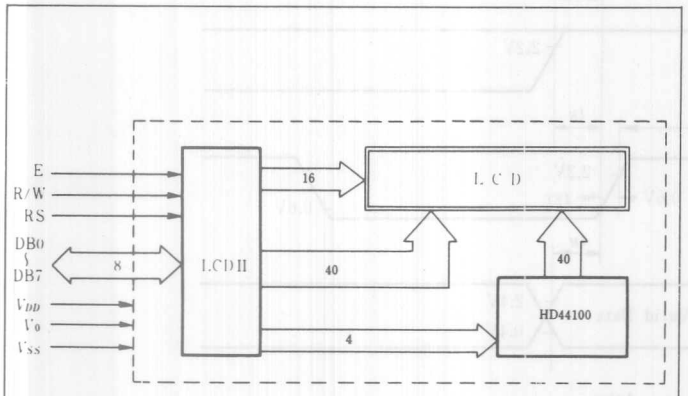


Fig. 3 Block diagram

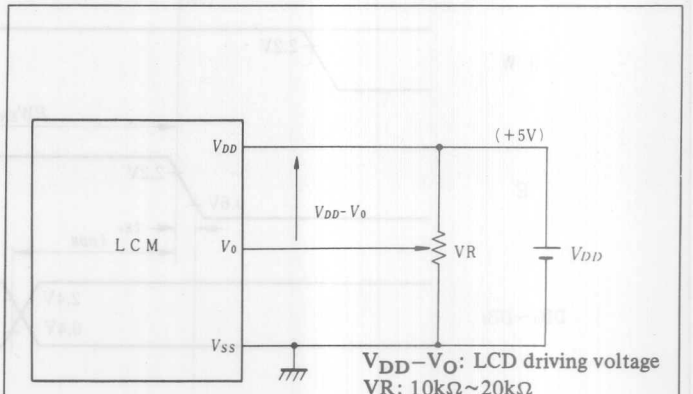


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

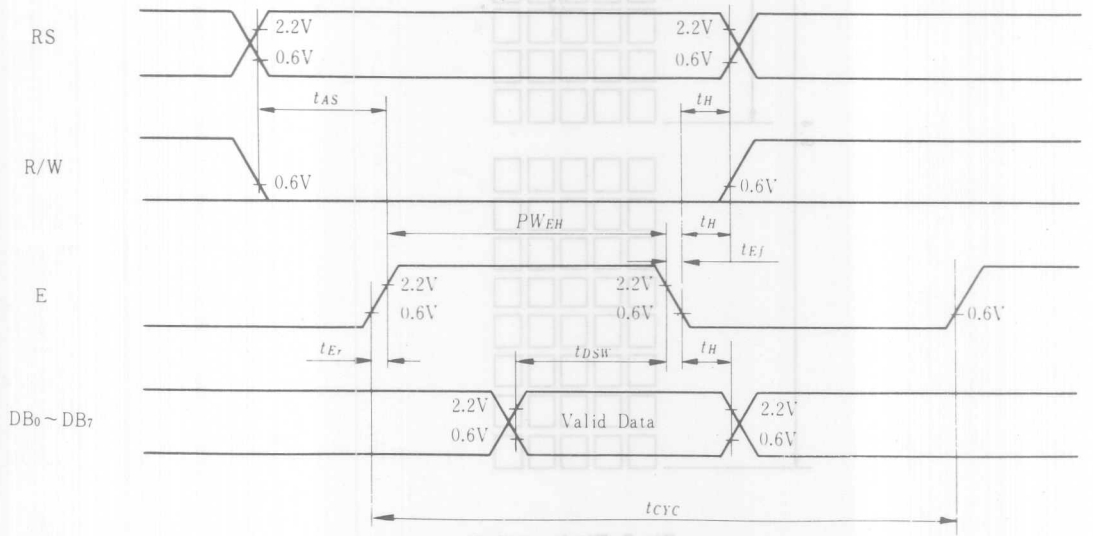


Fig. 5 Interface timing (data write)

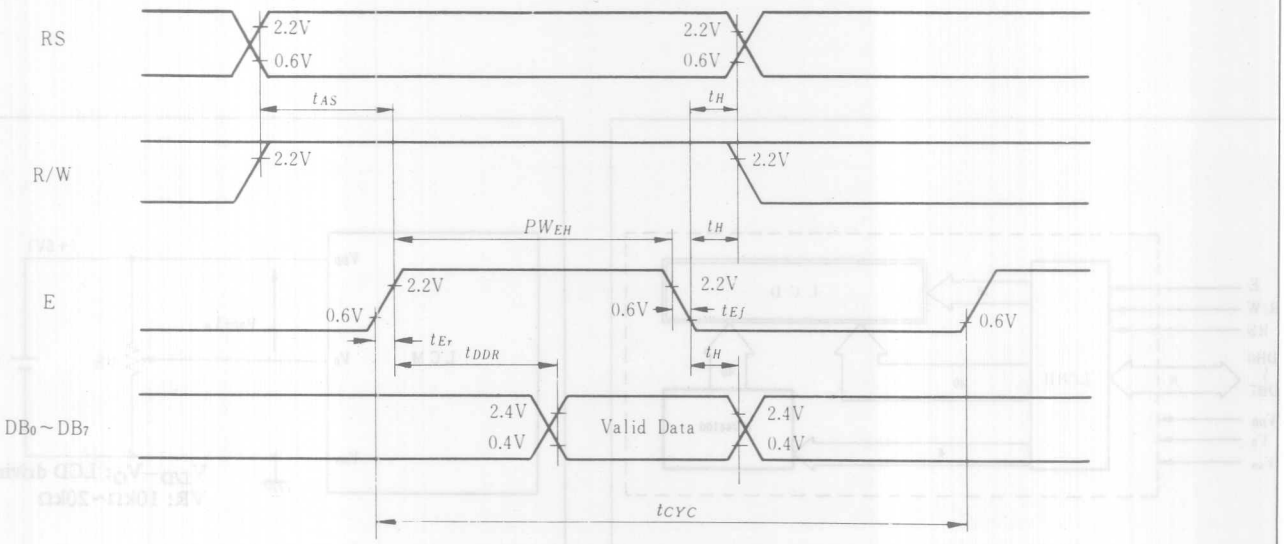


Fig. 6 Interface timing (data read)

LM016L

- 16 character x 2 lines
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	84W x 44H x 12T (max.) mm
Effective display area	61W x 15.8H mm
Character size (5 x 7 dots)	2.96W x 4.86H mm
Character pitch	3.55 mm
Dot size	0.56W x 0.66H mm
Weight	about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temeprature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ. 3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$) Duty = 1/16	
Ta = 0°C	4.6 V typ.
Ta = 25°C	4.4 V typ.
Ta = 50°C	4.2 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

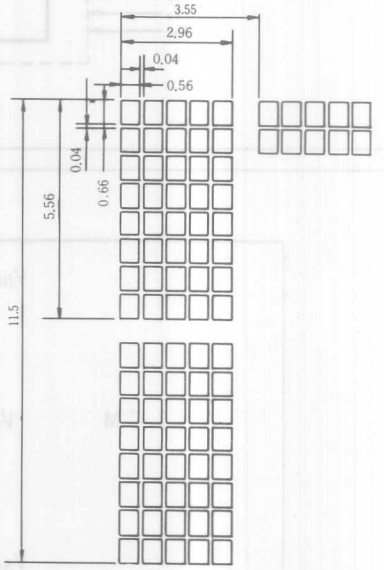


Fig. 1 Display pattern

Unit: mm

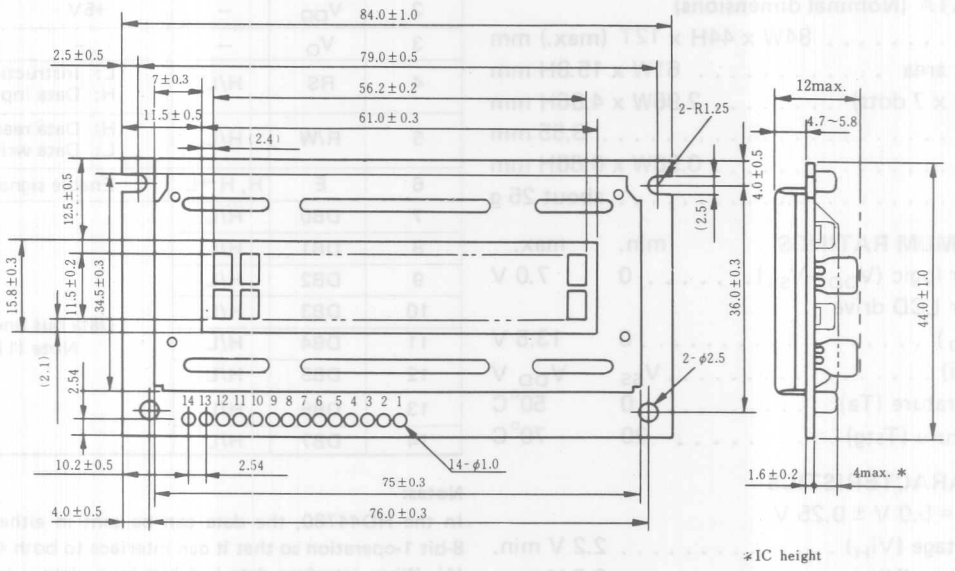


Fig. 2 External dimensions

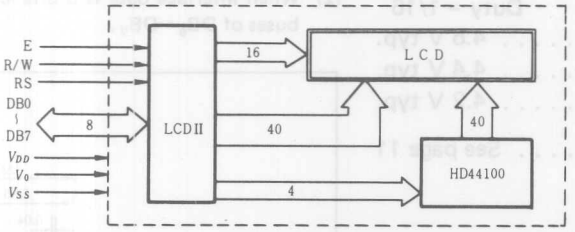
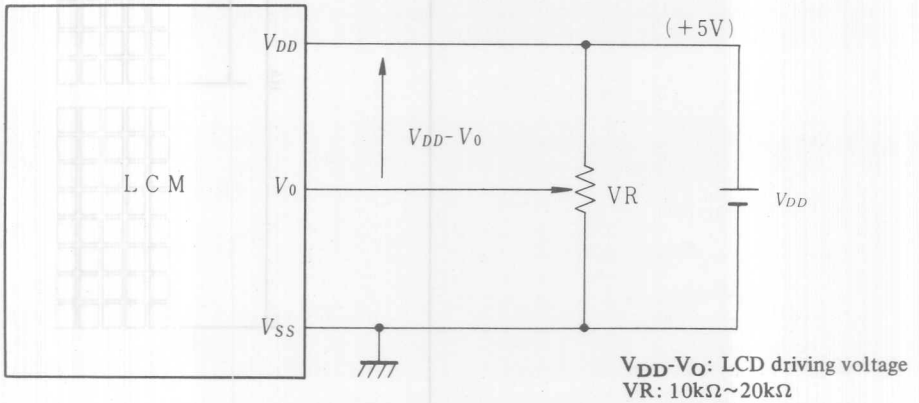


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

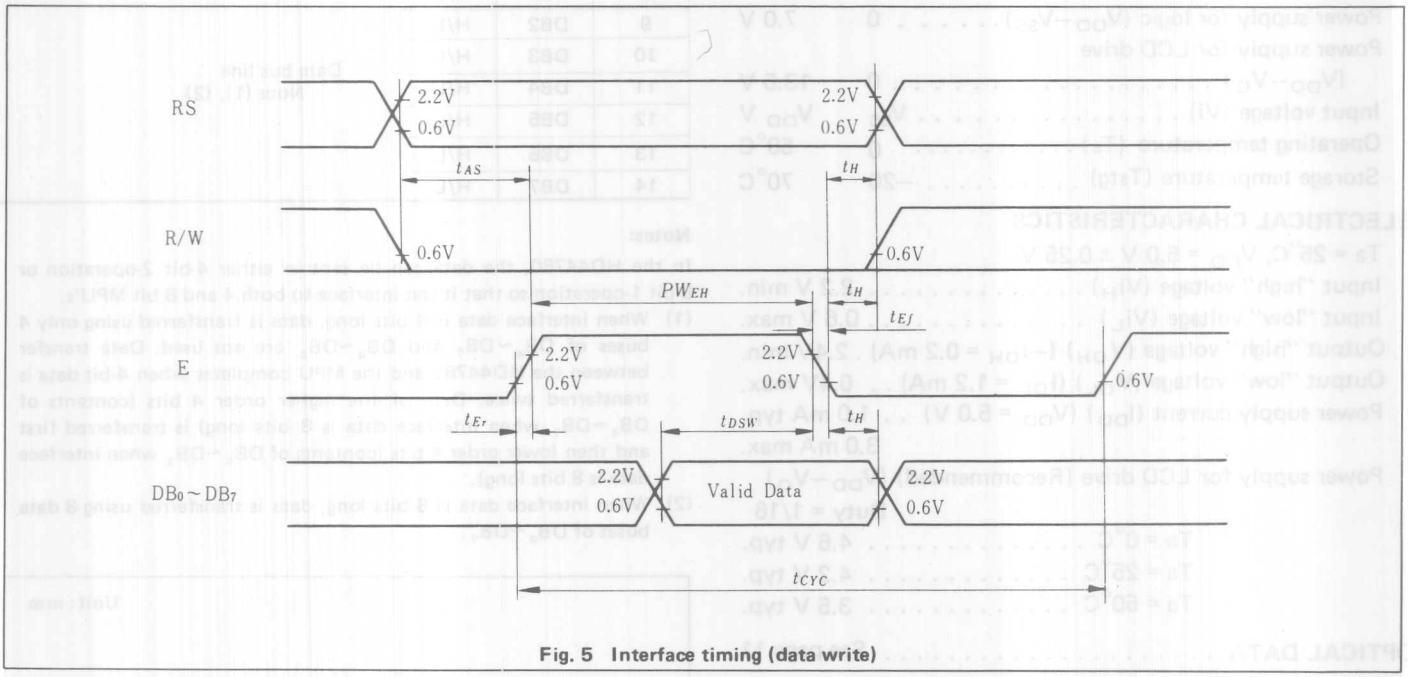


Fig. 5 Interface timing (data write)

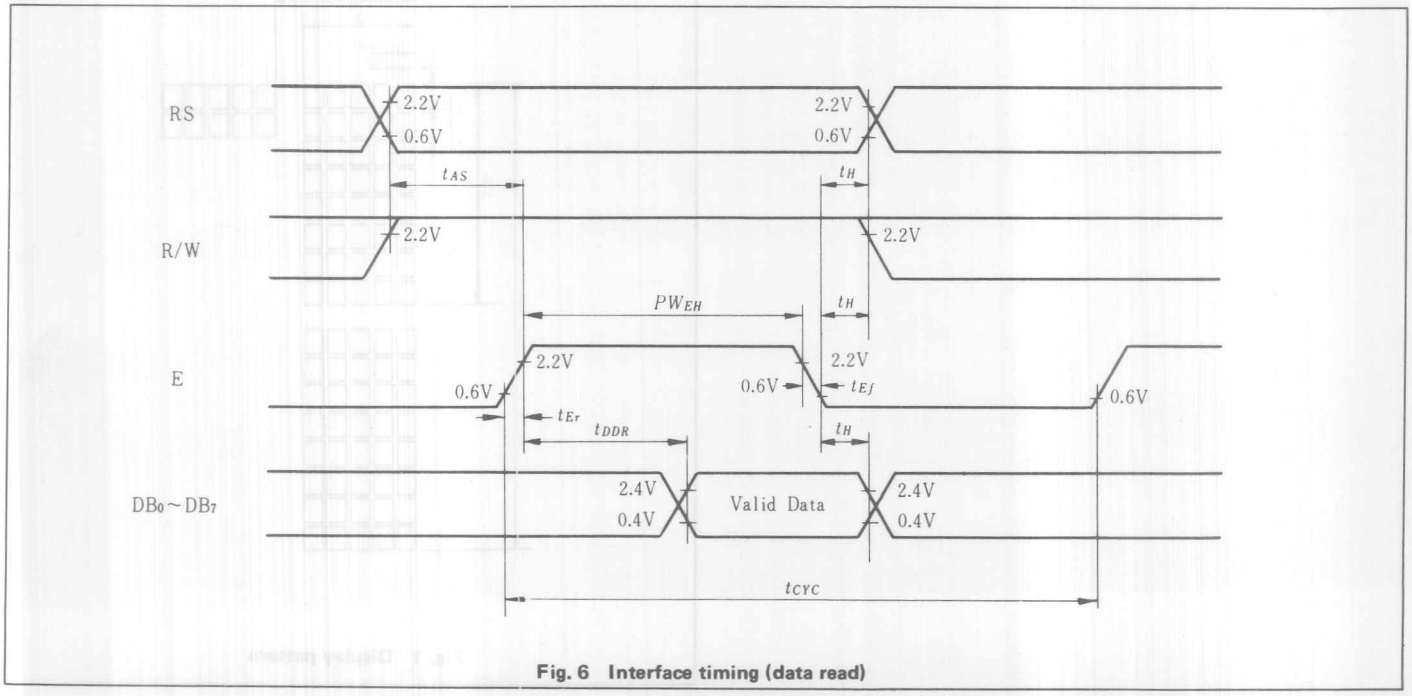


Fig. 6 Interface timing (data read)

LM032L

- 20 character x 2 lines
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 116W x 39H (max.) x 13T (max.) mm
Effective display area . . . . . 83W x 18.6H mm
Character size (5 x 7 dots) . . . . . 3.2W x 4.85H mm
Character pitch . . . . . 3.7 mm
Dot size . . . . . 0.6W x 0.65H mm
Weight . . . . . about 50 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V
Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . 2.4V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA) . . 0.4V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta = 0°C . . . . . 4.6 V typ.
Ta = 25°C . . . . . 4.2 V typ.
Ta = 50°C . . . . . 3.5 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	—	0V	Power supply
2	V_{DD}	—	+5V	
3	V_O	—	—	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of $DB_4 \sim DB_7$ and $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of $DB_0 \sim DB_3$ when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of $DB_0 \sim DB_7$.

Unit: mm

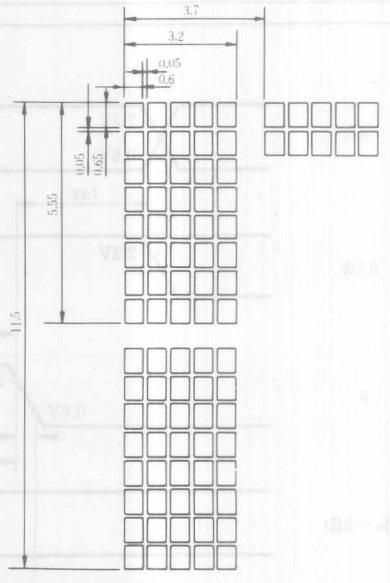


Fig. 1 Display pattern

Unit: mm

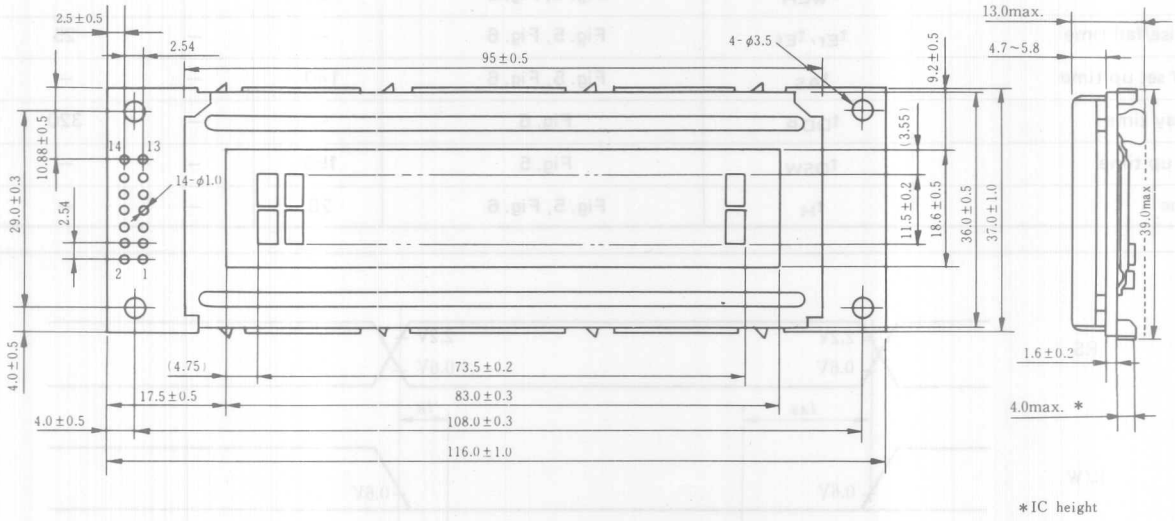


Fig. 2 External dimensions

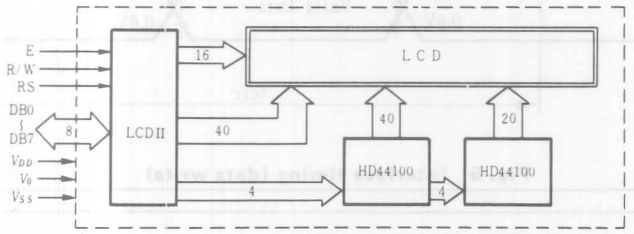
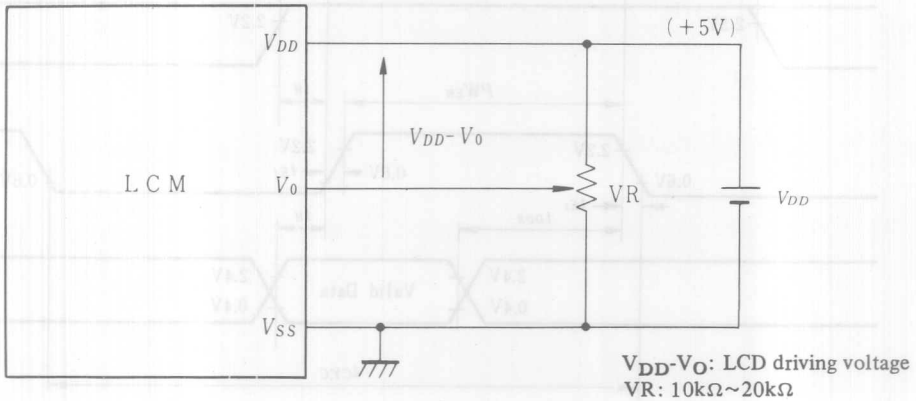


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

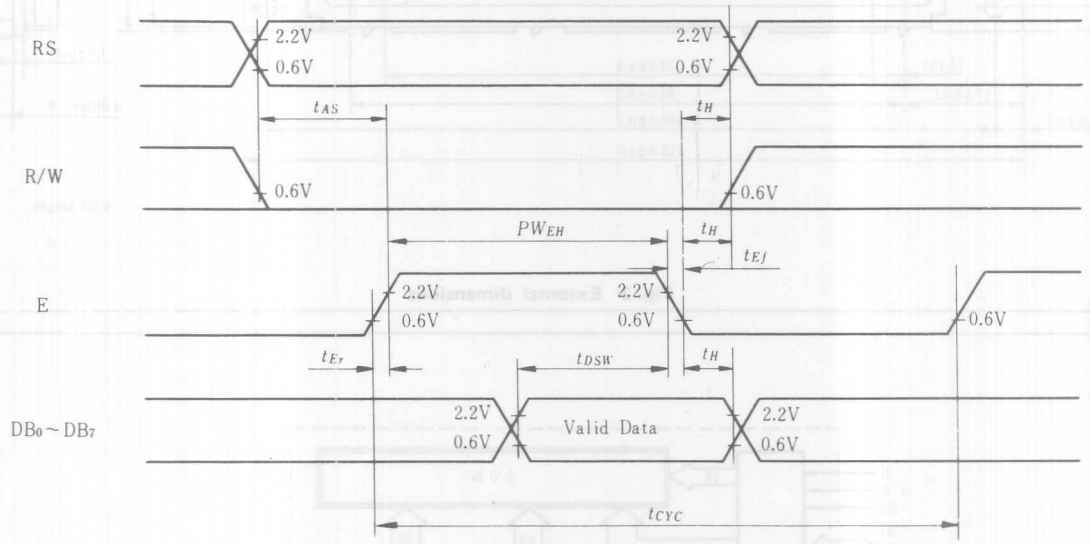


Fig. 5 Interface timing (data write)

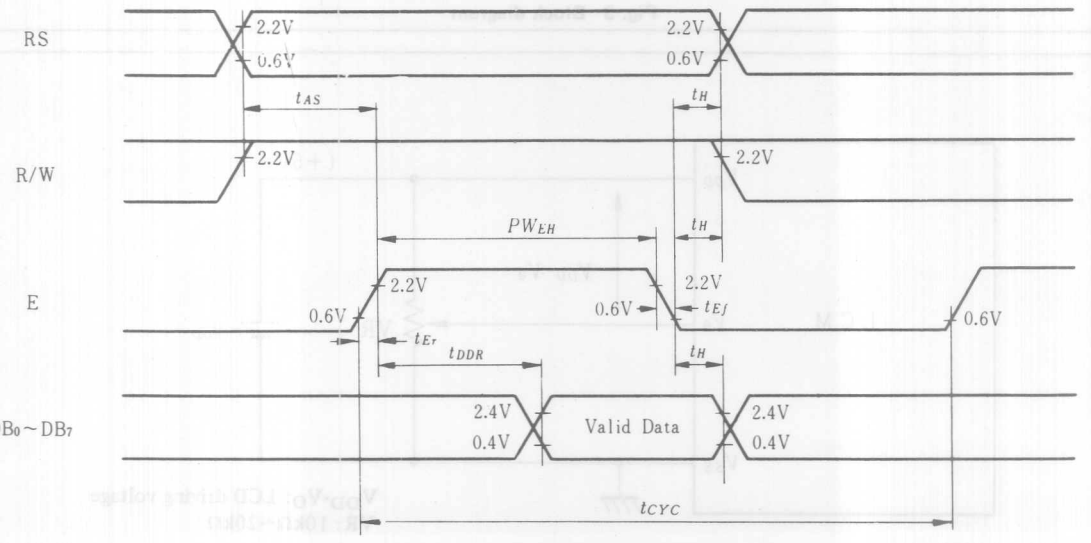


Fig. 6 Interface timing (data read)

LM060L

- 24 character x 2 lines
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 116W x 39H (max.) x 13T (max.) mm
Effective display area . . . . . 83W x 18.6H mm
Character size (5 x 7 dots) . . . . . 2.7W x 4.85H mm
Character pitch . . . . . 3.2 mm
Dot size . . . . . 0.5W x 0.65H mm
Dot pitch . . . . . 0.55W x 0.7H mm
Weight . . . . . about 50 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) 2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA) . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 2.0 mA typ.
3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta = 0°C . . . . . 4.6 V typ.
Ta = 25°C . . . . . 4.4 V typ.
Ta = 50°C . . . . . 3.2 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	V_{SS}	—	0V — Power supply
2	V_{DD}	—	+5V — Power supply
3	V_O	—	— — Power supply
4	RS	H/L	L: Instruction code input H: Data input
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)
6	E	H, H→L	Enable signal
7	DB0	H/L	Data bus line Note (1), (2)
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

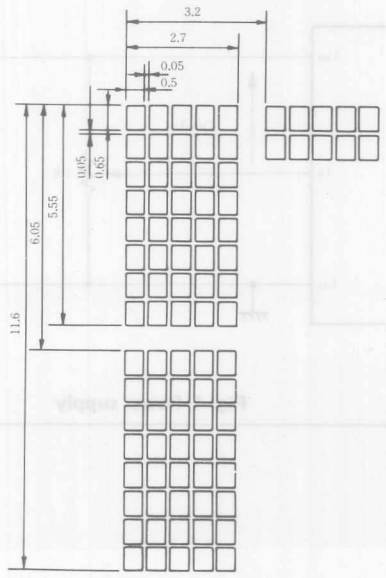


Fig. 1 Display pattern

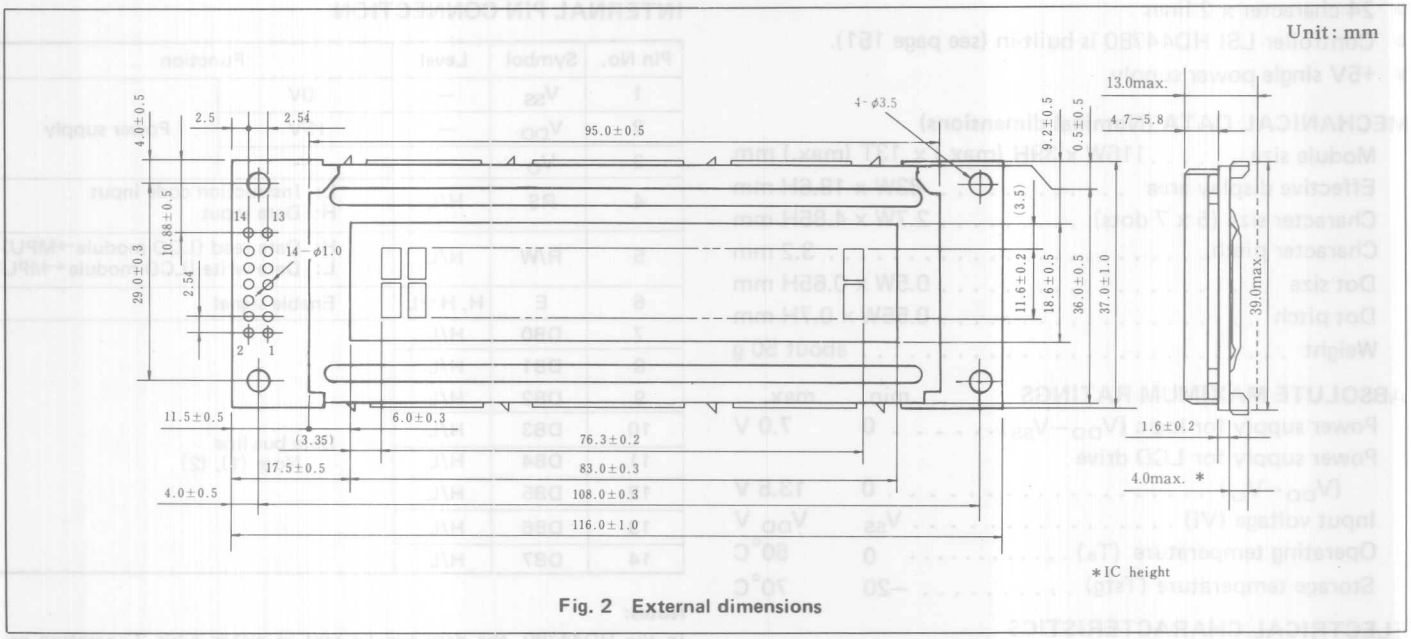


Fig. 2 External dimensions

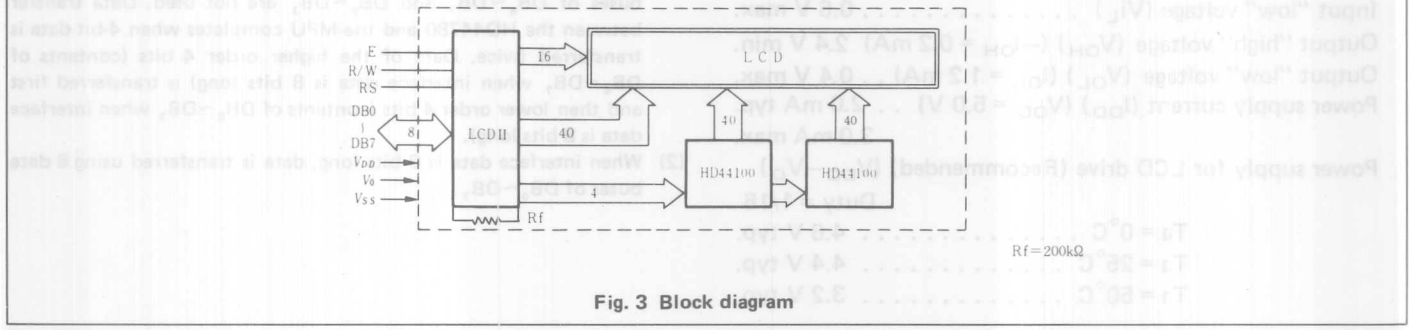
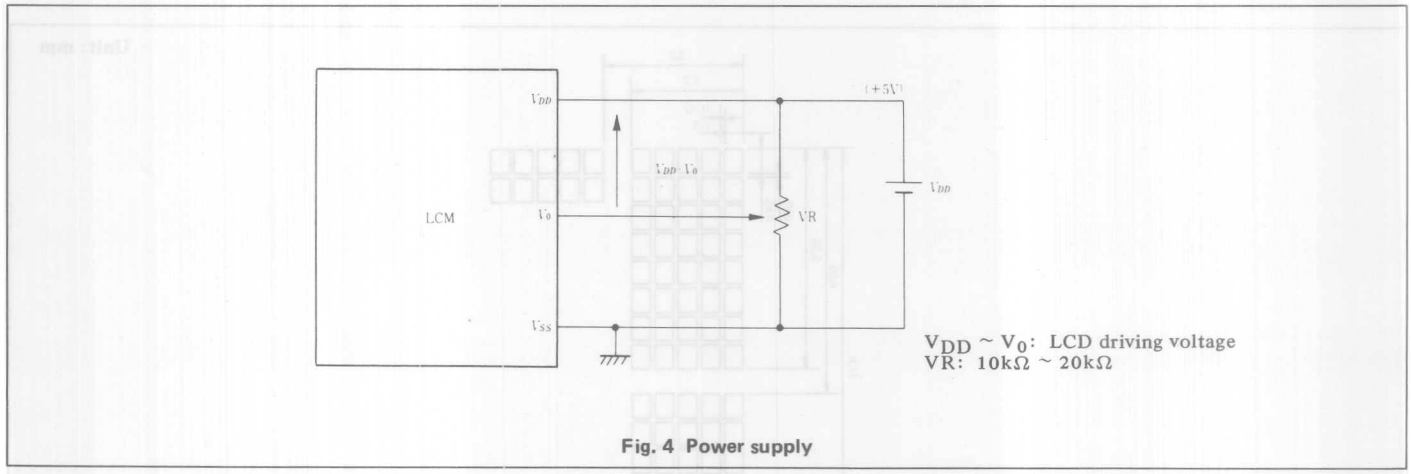


Fig. 3 Block diagram



$V_{DD} \sim V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

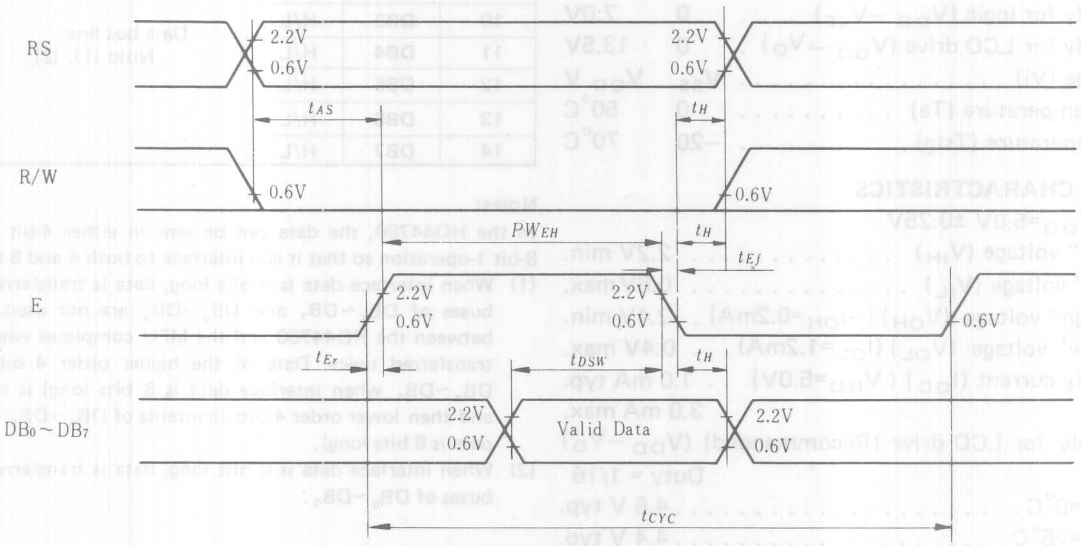


Fig. 5 Interface timing (data write)

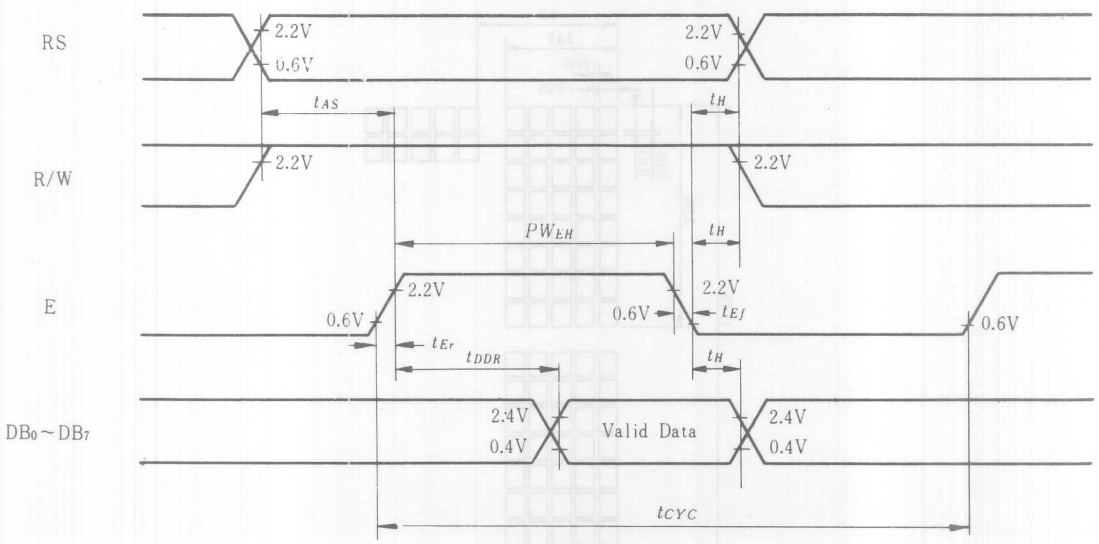


Fig. 6 Interface timing (data read)

LM017L

- 32 character x 2 lines
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . 174.5W x 33H (max.) x 13.4T (max.) mm
Effective display area . . . . . 141.19W x 16.75H mm
Character size (5 x 7 dots) . . . . . 3.45W x 4.85H mm
Character pitch . . . . . 4.2 mm
Dot size . . . . . 0.65W x 0.65H mm
Weight . . . . . about 60g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
power supply for LCD drive ($V_{DD}-V_O$) .	0	13.5V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V ±0.25V
Input "high" voltage (V_{IH}) . . . . . 2.2V min.
Input "low" voltage (V_{IL}) . . . . . 0.6V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$=0.2mA) . 2.4V min.
Output "low" voltage (V_{OL}) (I_{OL}=1.2mA) . . . 0.4V max.
Power supply current (I_{DD}) (V_{DD}=5.0V) . . 1.0 mA typ.
3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta=0°C . . . . . 4.6 V typ.
Ta=25°C . . . . . 4.4 V typ.
Ta=50°C . . . . . 4.2 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

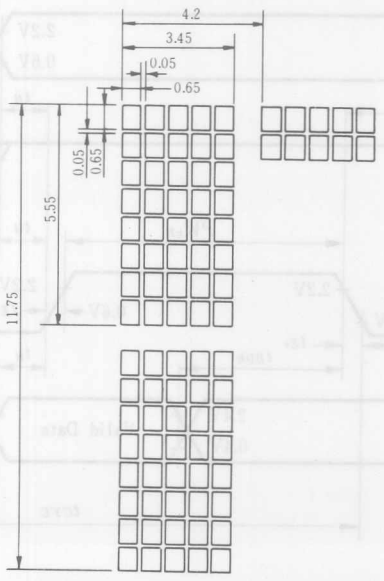


Fig. 1 Display pattern

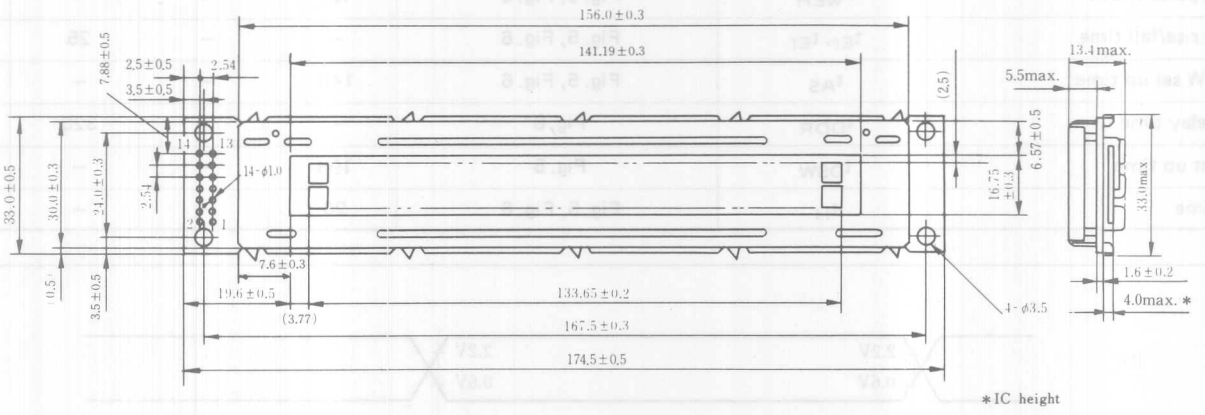


Fig. 2 External dimensions

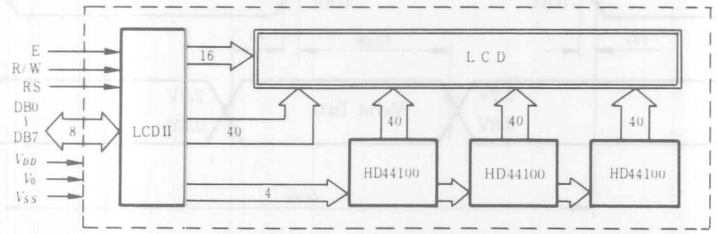


Fig. 3 Block diagram

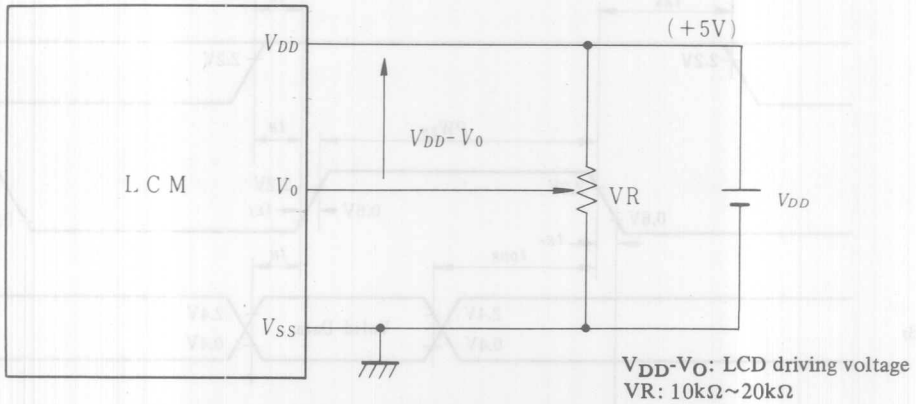


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

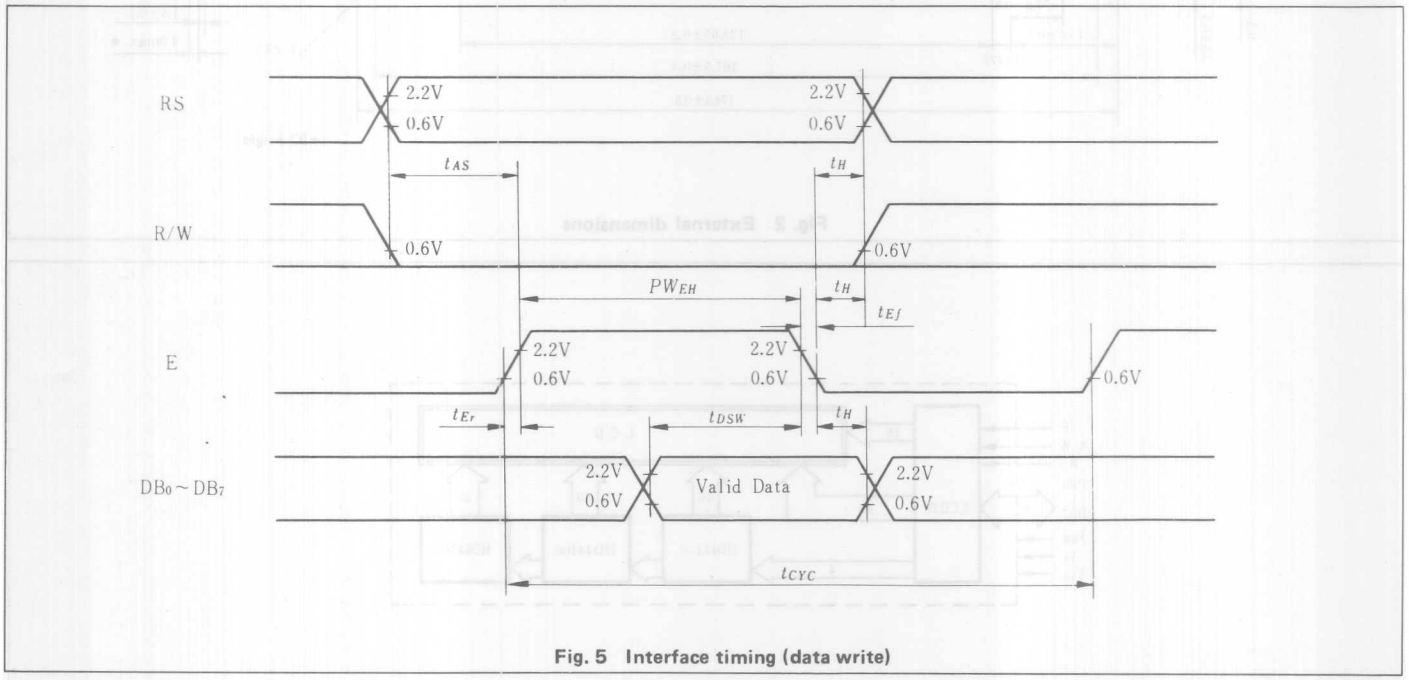


Fig. 5 Interface timing (data write)

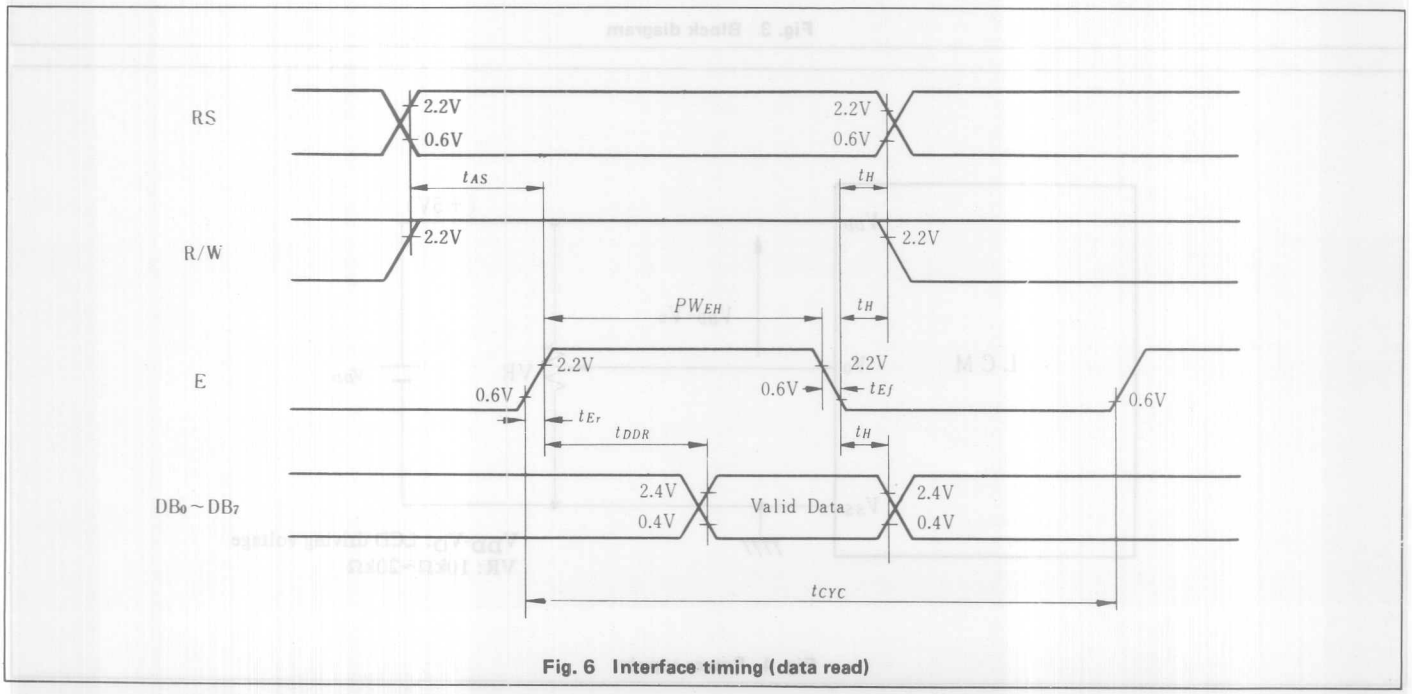


Fig. 6 Interface timing (data read)

LM018L

- 40 character x 2 lines
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . 182W x 35.5H (max.) x 13T (max.) mm
Effective display area . . . . . 154.0W x 15.3H mm
Character size (5 x 7 dots) . . . . . 3.2W x 4.85H mm
Character pitch . . . . . 3.7 mm
Dot size . . . . . 0.6W x 0.65H mm
Weight . . . . . about 65g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V ±0.25V
Input "high" voltage (V_{IH}) . . . . . 2.2V min.
Input "low" voltage (V_{IL}) . . . . . 0.6V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$=0.2mA). . 2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL}=1.2mA) . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD}=5.0V) . . . 1.0 mA typ.
3.0mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta=0°C . . . . . 4.6 V typ.
Ta=25°C . . . . . 4.4 V typ.
Ta=50°C . . . . . 4.2 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	V_{SS}	—	0V
2	V_{DD}	—	+5V
3	V_O	—	—
4	RS	H/L	L: Instruction code input H: Data input
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)
6	E	H, H→L	Enable signal
7	DB0	H/L	Data bus line Note (1), (2)
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

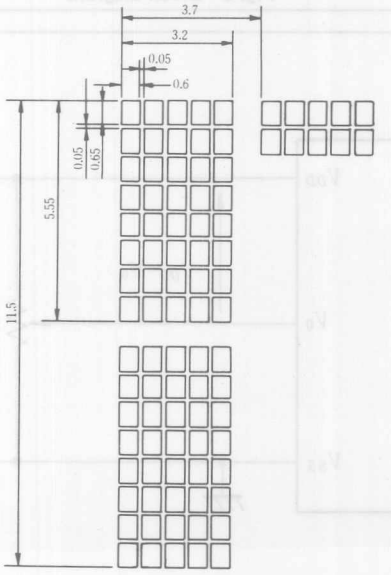


Fig. 1 Display pattern

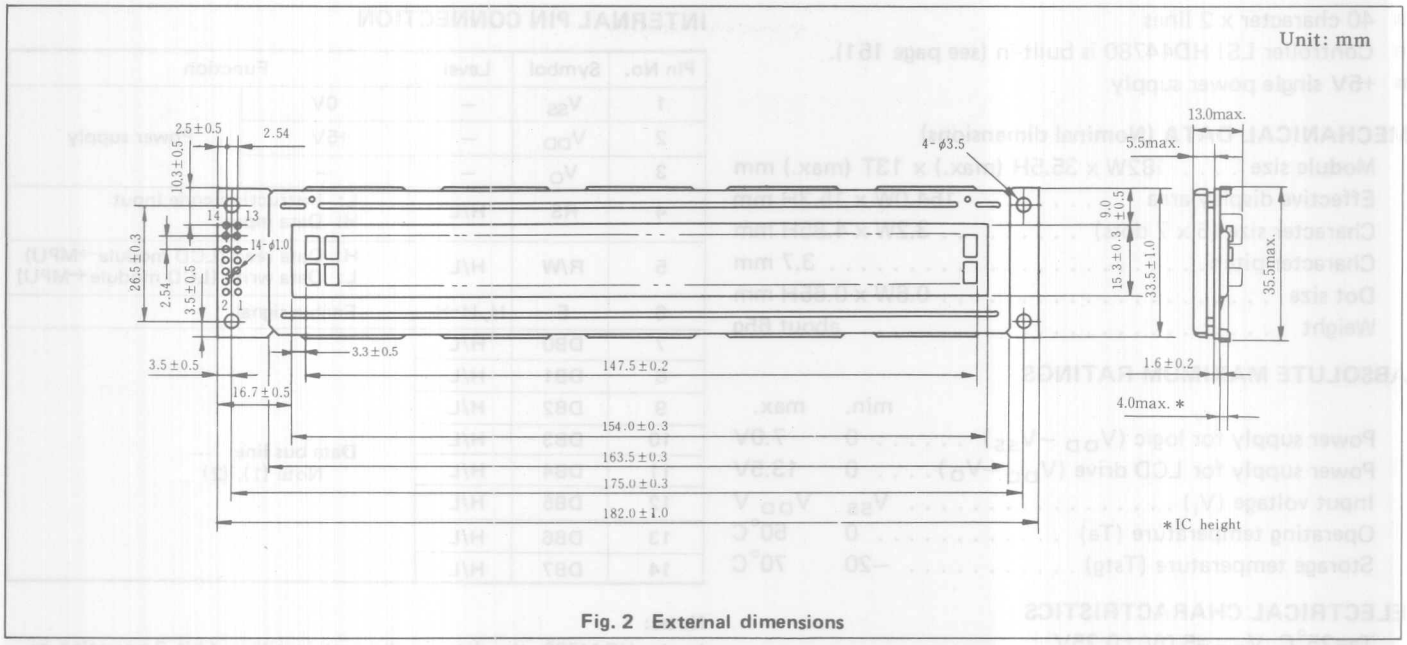


Fig. 2 External dimensions

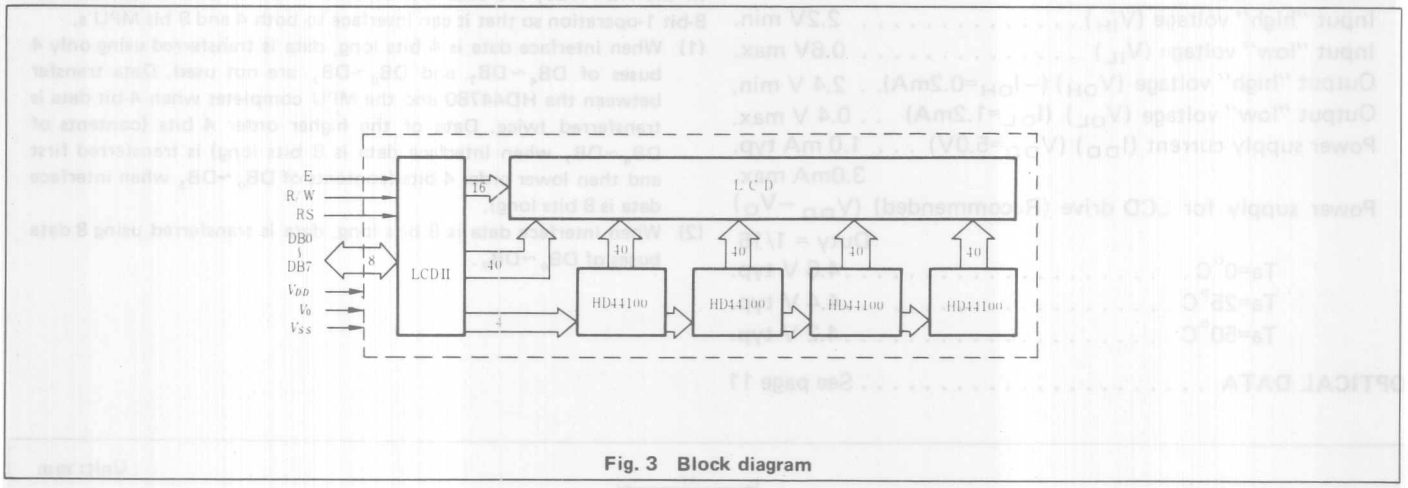


Fig. 3 Block diagram

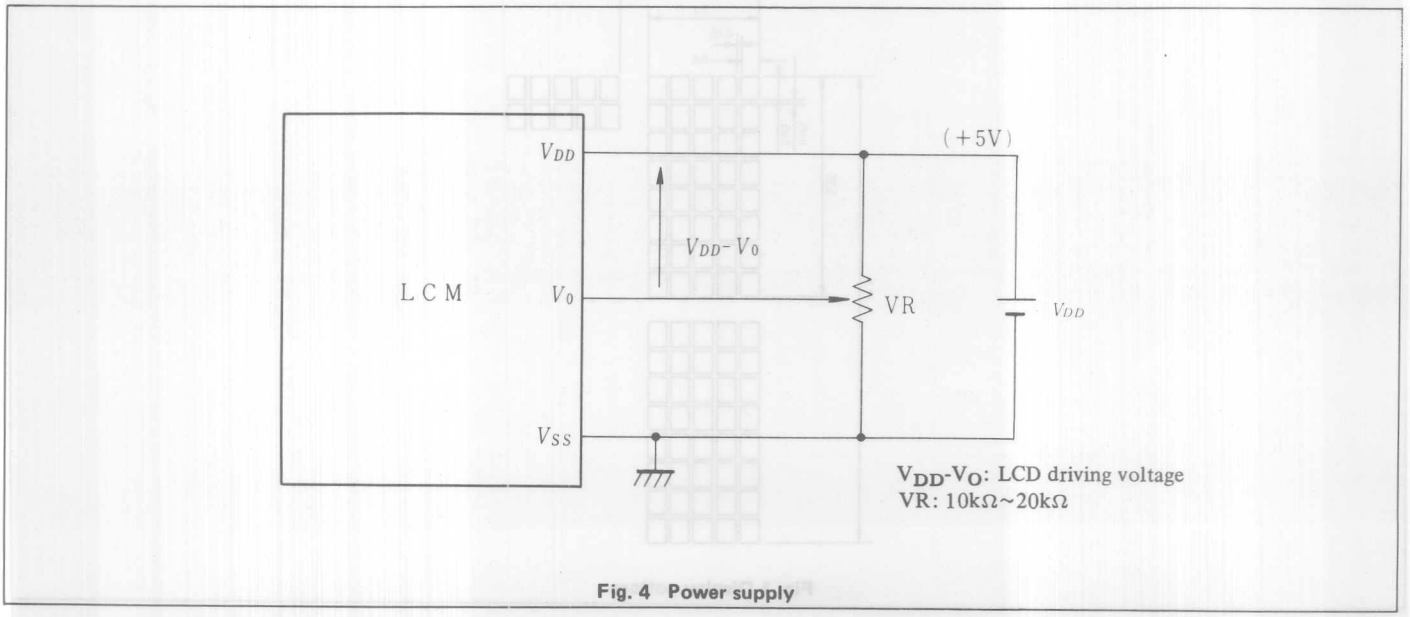


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

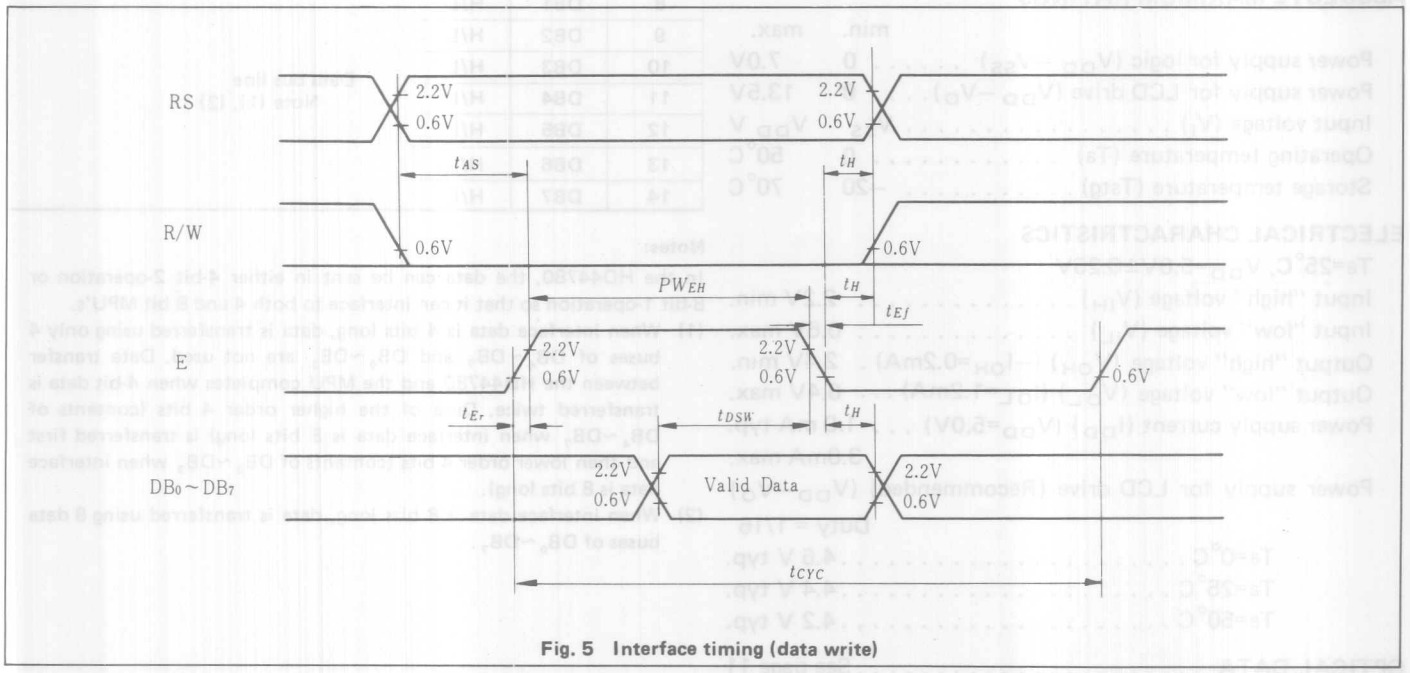


Fig. 5 Interface timing (data write)

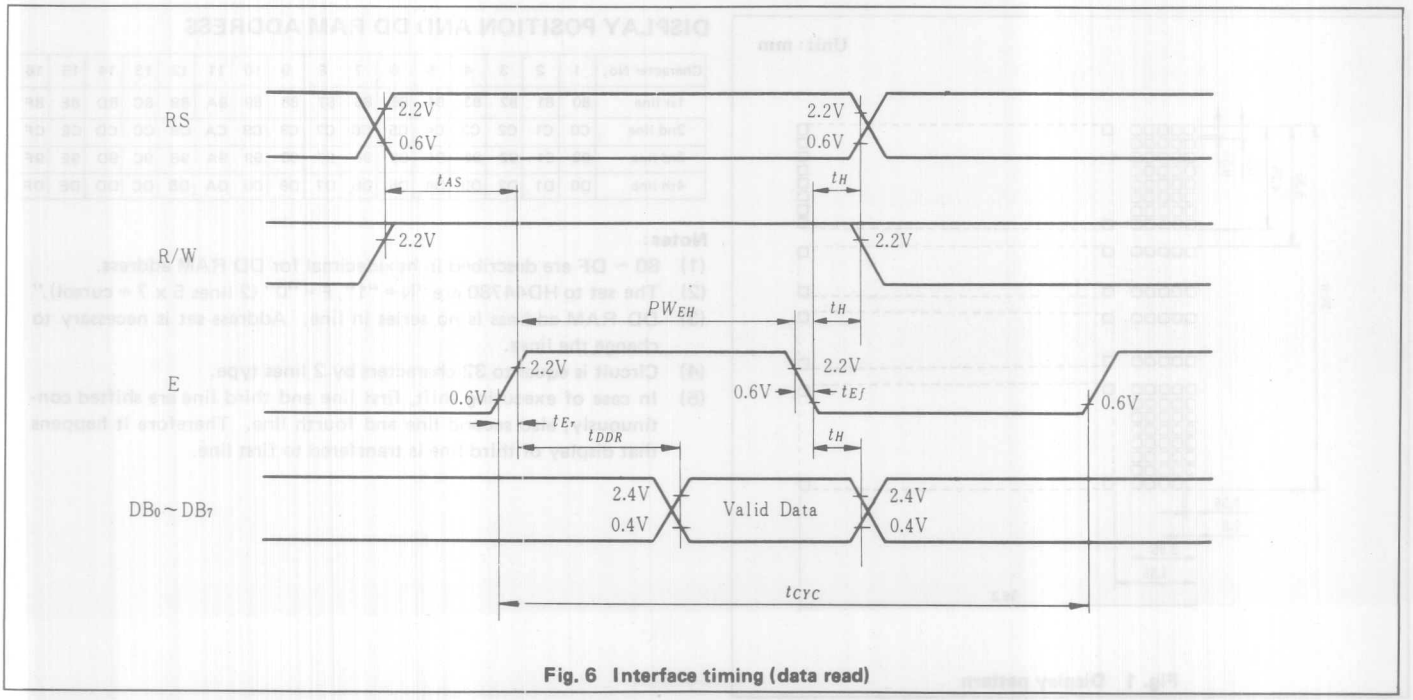


Fig. 6 Interface timing (data read)

LM041L

- 16 character x 4 lines
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	87W x 60H x 12T (max.) mm
Effective display area	61.8W x 25.2H mm
Character size (5 x 7 dots)	2.95W x 4.15H mm
Character pitch	3.55 mm
Dot size	0.55W x 0.55H mm
Weight	about 60g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V

Input "high" voltage (V_{IH})	2.2V min.
Input "low" voltage (V_{IL})	0.6V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$=0.2mA)	2.4V min.
Output "low" voltage (V_{OL}) (I_{OL}=1.2mA)	0.4V max.
Power supply current (I_{DD}) (V_{DD}=5.0V)	1.0 mA typ.
	3.0mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)	
	Duty = 1/16
Ta=0°C	4.6 V typ.
Ta=25°C	4.4 V typ.
Ta=50°C	4.2 V typ.

OPTICAL DATA ..... See page 11

Unit: mm

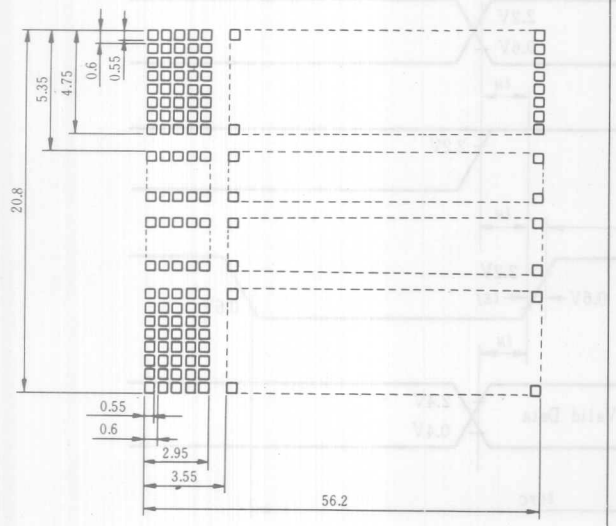


Fig. 1 Display pattern

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	—	0V	Power supply
2	V_{DD}	—	+5V	
3	V_O	—	—	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

DISPLAY POSITION AND DD RAM ADDRESS

Character No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
2nd line	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF
3rd line	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
4th line	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF

Notes:

(1) 80 ~ DF are described in hexidecimal for DD RAM address.

(2) The set to HD44780 are "N = "1", F = "0" (2 lines 5 x 7 + cursol)."

(3) DD RAM address is no series in line. Address set is necessary to change the lines.

(4) Circuit is equal to 32 characters by 2 lines type.

(5) In case of executing shift, first line and third line are shifted continuously, also second line and fourth line. Therefore it happens that display of third line is transfered to first line.

Unit: mm

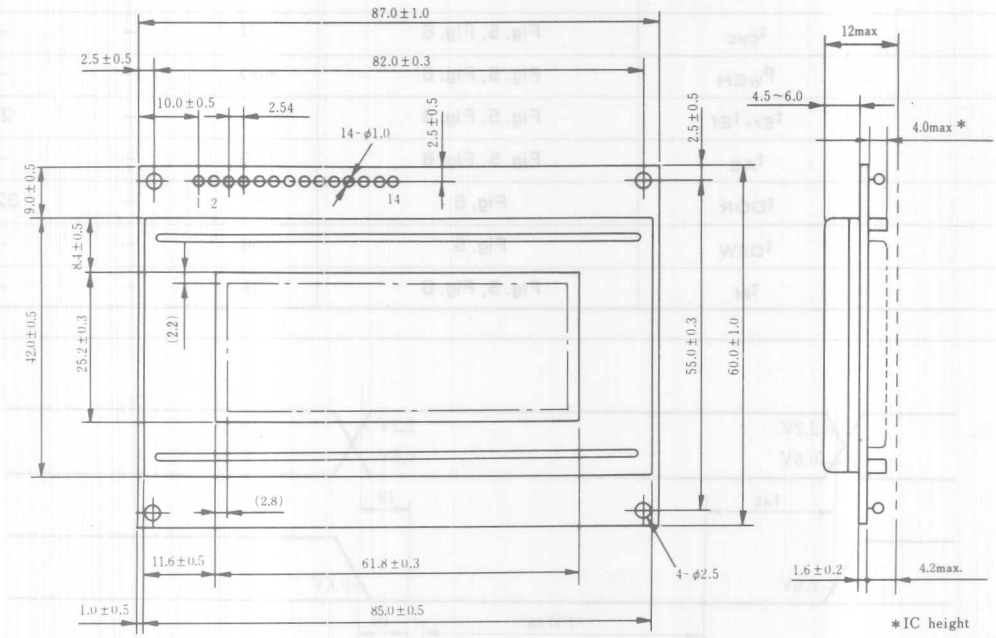


Fig. 2 External dimensions

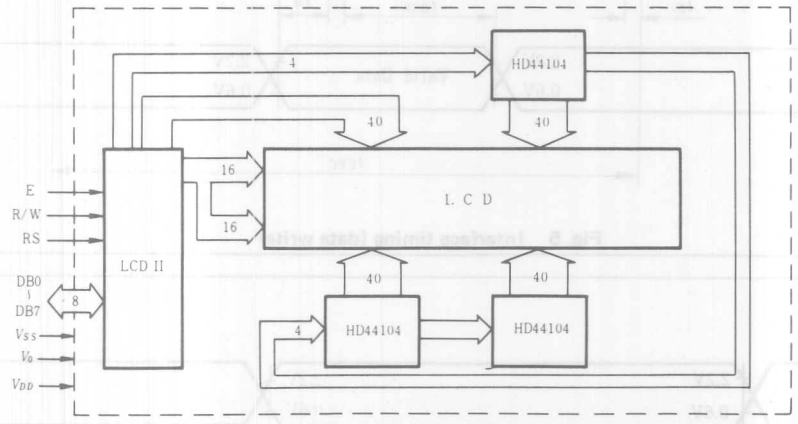
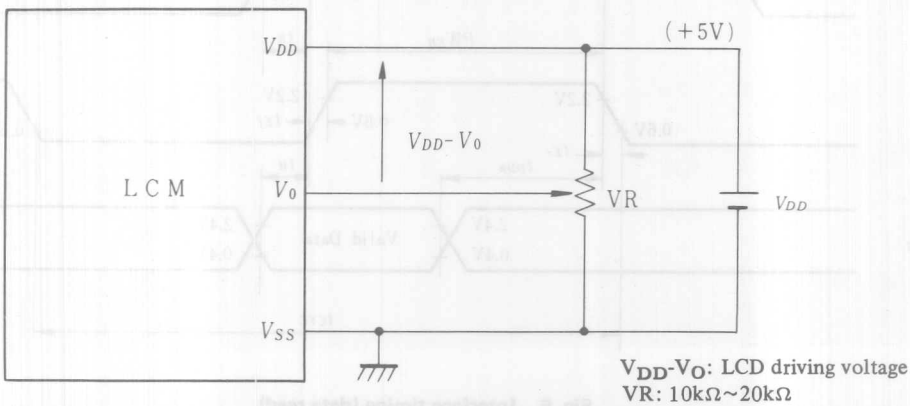


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

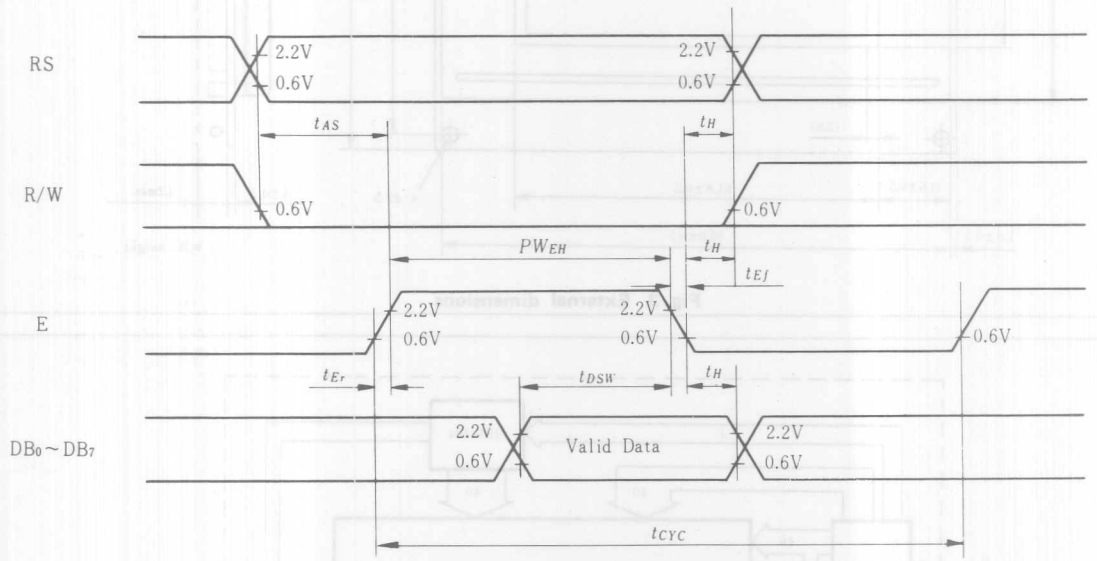


Fig. 5 Interface timing (data write)

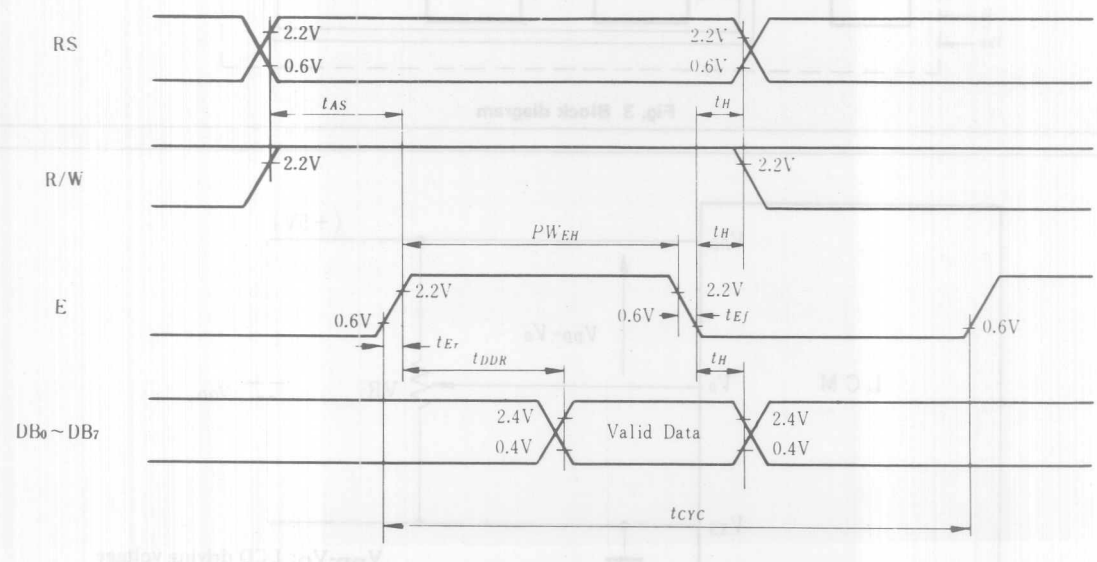


Fig. 6 Interface timing (data read)

LM044L

- 20 character x 4 lines
- Controller LSI HD44780 is built-in (see page 151).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	98W x 60H x 12T (max.) mm
Effective display area	76.0W x 25.2H mm
Character size (5 x 7 dots)	2.95W x 4.15H mm
Character pitch	3.55 mm
Dot size	0.55W x 0.55H mm
Weight	about 65 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ. 3.5 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$) Duty = 1/16	
Ta = 0°C	4.6 V typ.
Ta = 25°C	4.4 V typ.
Ta = 50°C	4.2 V typ.

OPTICAL DATA ..... See page 11

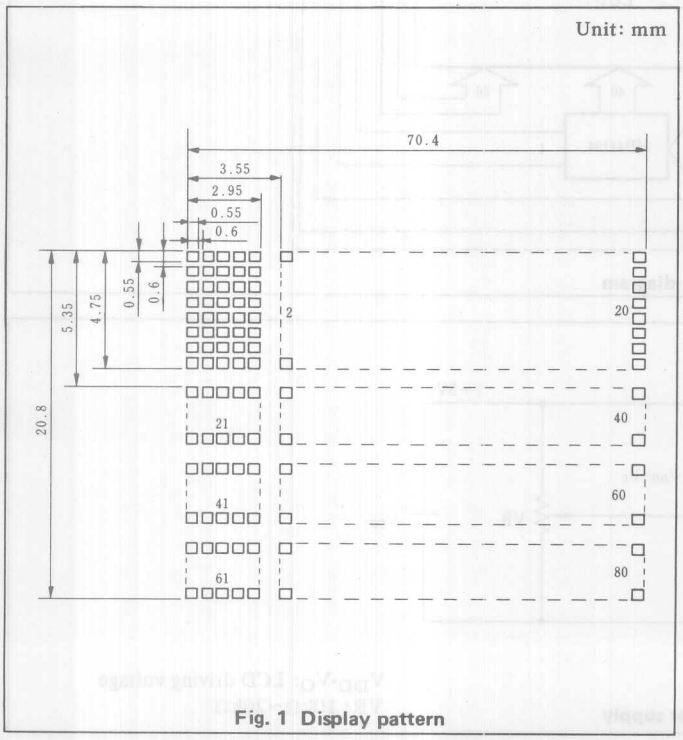


Fig. 1 Display pattern

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	V_{SS}	–	0V (Power supply)
2	V_{DD}	–	+5V (Power supply)
3	V_O	–	– (Power supply)
4	RS	H/L	L: Instruction code input H: Data input
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)
6	E	H, H→L	Enable signal
7	DB0	H/L	Data bus line Note (1), (2)
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

DISPLAY POSITION AND DD RAM ADDRESS

Character No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1st line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93
2nd line	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3
3rd line	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7
4th line	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7

Notes:

(1) 80 ~ E7 are described in hexidecimal for DD RAM address.

(2) The set to HD44780 are "N = "1", F = "0" (2 lines 5 x 7 + cursol)."

(3) DD RAM address is no series in line. Address set is necessary to change the lines.

(4) Circuit is equal to 40 characters by 2 lines type.

(5) In case of executing shift, first line and third line are shifted continuously, also second line and fourth line. Therefore it happens that display of third line is transfered to first line.

Unit: mm

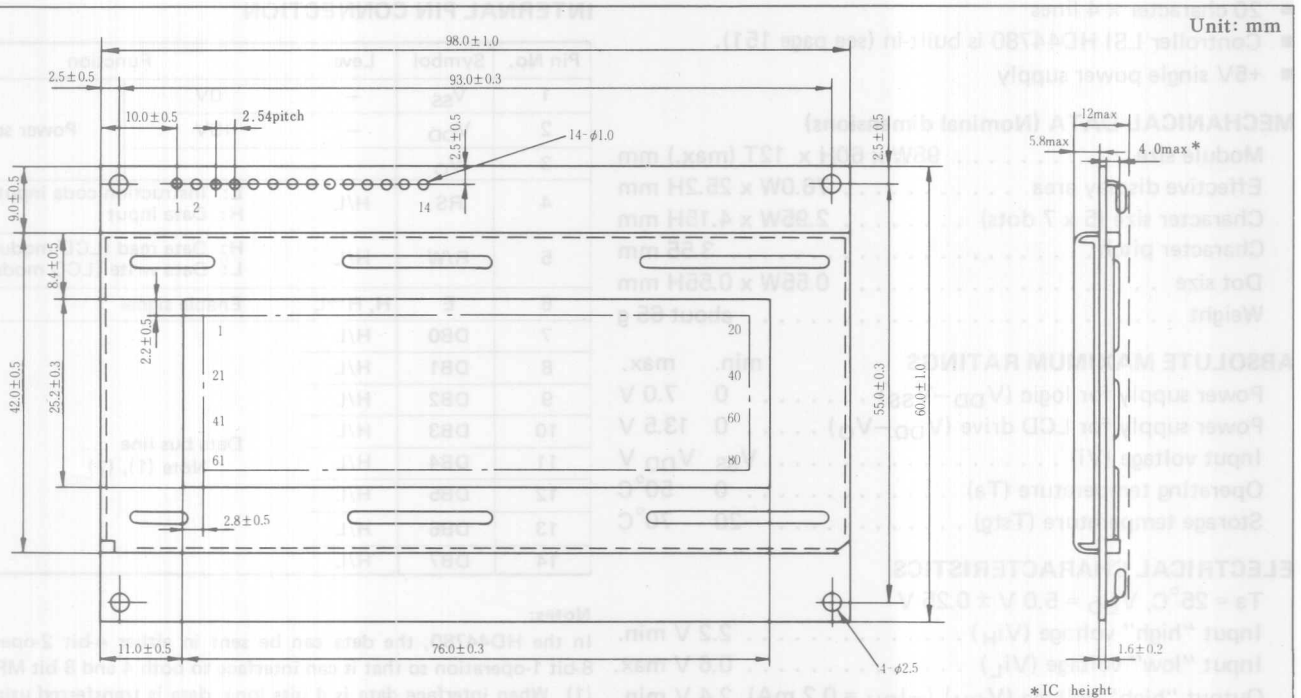


Fig. 2 External dimension

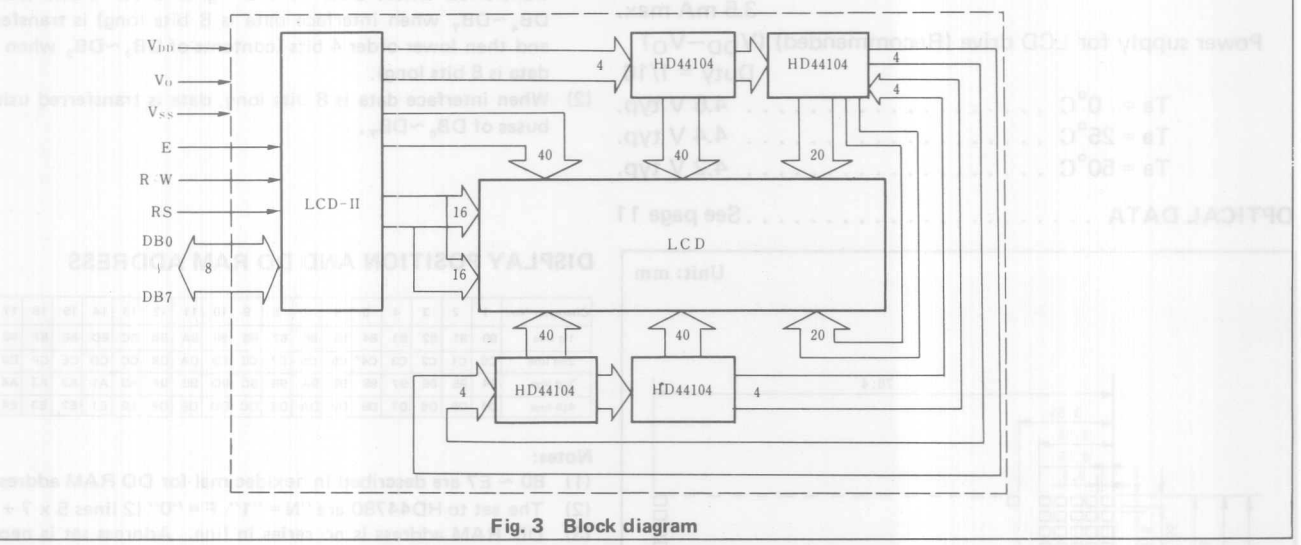
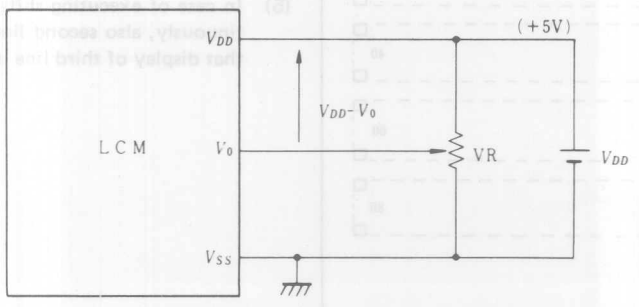


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

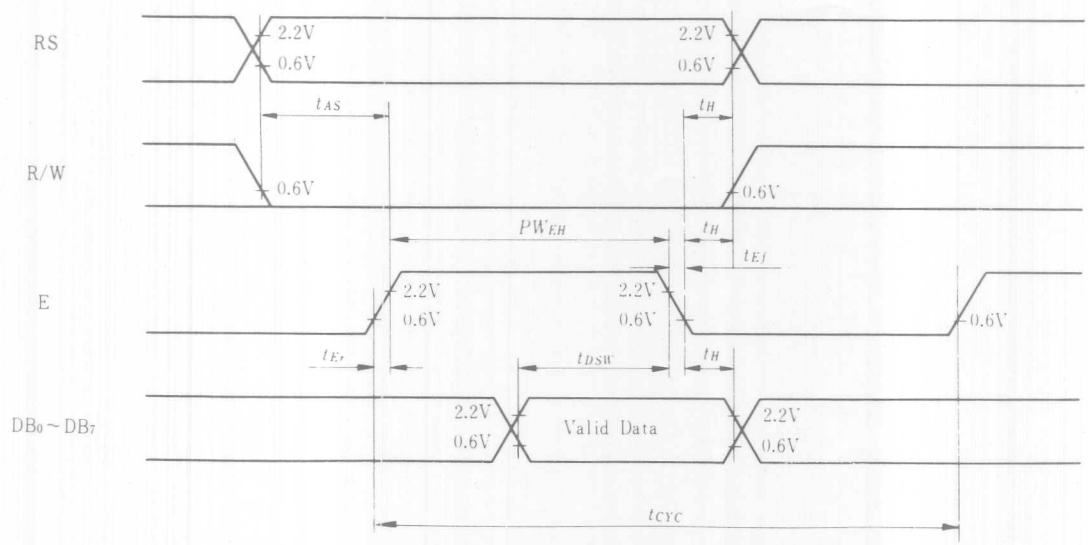


Fig. 5 Interface timing (data write)

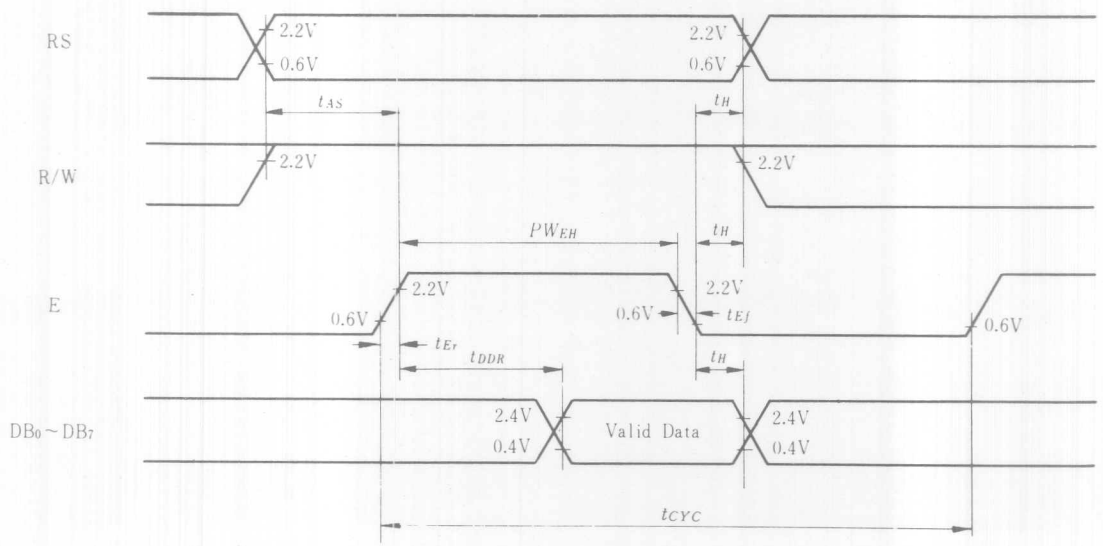


Fig. 6 Interface timing (data read)

LCD MODULE WITH ATTACHABLE CONTROLLER LSI

This module consists of LCD device, driver LSI, PC board, and other parts.
By attaching the controller LSI HD43160A, numerals, alphabets, Kana, and symbols can be displayed.

Controller LSI HD43160AH for LCD Module

H2532A	(16 x 1 line)
H2535	(16 x 2 lines)
H2538A	(40 x 1 line)
H2539	(40 x 2 lines)

CONTROLLER LSI HD43160AH FOR LCD MODULE

- Controller with built-in character generator
- Applicable type: H2532 · H2535 · H2538A · H2539

The HD43160AH receives character data written in the ASCII code or JIS code from microcomputer and stores them in its RAM which has 80 words capacity.

The HD43160AH converts these data into serial character pattern, then transfers them to LCD drivers.
It also generates other signals for LCD.

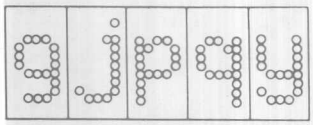
1. CHARACTER DISPLAY

- Alphanumeric character; A ~ Z, a ~ z, @, #, %, &, etc.
- Japanese Character (katakana)
- 160 characters by internal character generator (ROM). (Max. 256 characters by external ROM)

2. CHARACTER DOT PATTERNS

- 5 x 7
  The bottom lines of the English small characters "g, i, p, q, y," are on the cursor line.

- 5 x 11
  Only English small character "g, j, p, q, y," are displayed as below, the others are in the same way as that of 5 x 7.

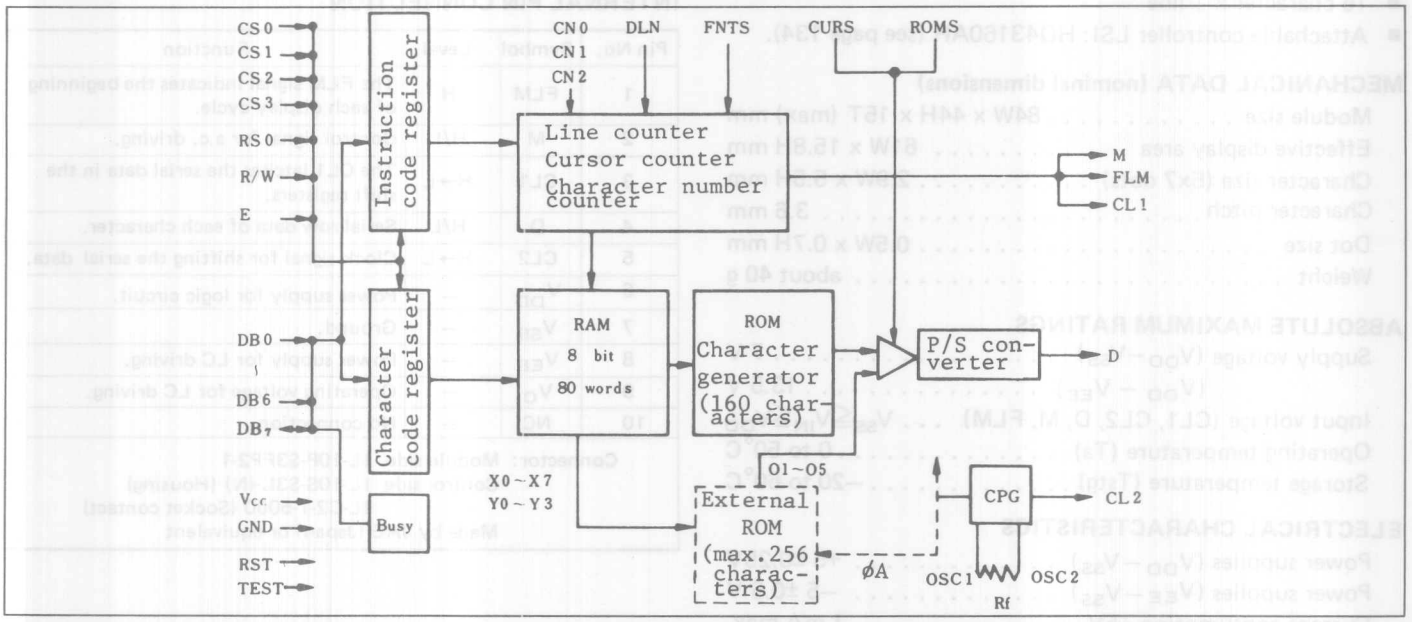


- Cursor 5 dots: ●●●●●
  1 dot : ●
  The cursor is displayed on the 8th or 12th line.

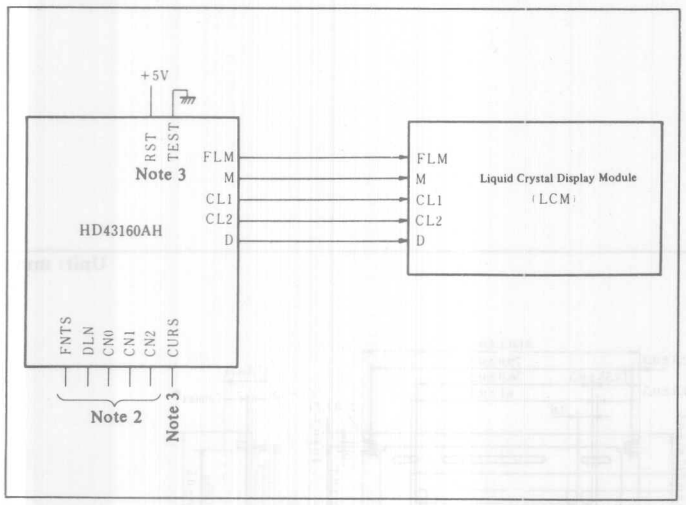
3. OTHER FUNCTION CONTROLLED BY MICROCOMPUTER

- Display clear
- Cursor ON/OFF
- Cursor position preset (Character position)
- Cursor return

4. BLOCK DIAGRAM



5. The HD43160A is a CMOS LSI developed to control the LCD module described below, and contains a character generator and character data memory.
Applied type: H2532A, H2535, H2538A, H2539, H2555, and H2568.
Example of a connection between HD43160AH and LCD module.



Note 1: When CURS = "1", the cursor has a 5 x 1 dot constitution. (■■■■■)
When CURS = "0", the cursor has a 1 x 1 dot constitution. (□□■□□)

Note 2: Treatment examples for all types are shown in the table below.

0: GND
1: V_{DD} (+5V)

Type No. \ Terminal	FNTS	DLN	CN0	CN1	CN2
H2532A	0	0	0	1	0
H2535	0	1	0	0	1
H2538A	0	0	1	0	1
H2539	0	1	1	1	1

Note 3: The test terminal is fixed at the "0" level.
The RST terminal is normally at the "1" level.
When set at the "0" level, oscillation is stopped and DC voltage is loaded to the liquid crystal.

H2532A

- 16 character x 1 line
- Attachable controller LSI: HD43160AH (see page 134).

MECHANICAL DATA (nominal dimensions)

Module size	84W x 44H x 15T (max) mm
Effective display area	61W x 15.8H mm
Character size (5x7 dots)	2.9W x 5.5H mm
Character pitch	3.6 mm
Dot size	0.5W x 0.7H mm
Weight	about 40 g

ABSOLUTE MAXIMUM RATINGS

Supply voltage ($V_{DD}-V_{SS}$)	7 V
($V_{DD}-V_{EE}$)	13.5 V
Input voltage (CL1, CL2, D, M, FLM)	$V_{SS} \leqq V_{IN} \leqq V_{DD}$
Operating temperature (Ta)	0 to 50°C
Storage temperature (Tstg)	−20 to 60°C

ELECTRICAL CHARACTERISTICS

Power supplies ($V_{DD}-V_{SS}$)	+5 ±0.25V
Power supplies ($V_{EE}-V_{SS}$)	−5 ±0.5 V
Current consumption +5V	1 mA max.
−5V	1 mA max.
Input high voltage	0.7 V_{DD} V min.
Input low voltage	0.3 V_{DD} V max.
Power supply for LCD drive (Recommended) (V_O-V_{EE})	
Ta = 0°C	5.3 V typ.
Ta = 25°C	4.5 V typ.
Ta = 50°C	3.7 V typ.

OPTICAL DATA ..... See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	FLM	H	The FLM signal indicates the beginning of each display cycle.
2	M	H/L	Control signal for a.c. driving.
3	CL1	H→L	The CL1 latches the serial data in the shift registers.
4	D	H/L	Serial row data of each character.
5	CL2	H→L	Clock signal for shifting the serial data.
6	V_{DD}	–	Power supply for logic circuit.
7	V_{SS}	–	Ground.
8	V_{EE}	–	Power supply for LC driving.
9	V_O	–	Operating voltage for LC driving.
10	NC	–	No connection.

Connector: Module side IL-10P-S3FP2-1
Control side IL-10S-S3L-(N) (Housing)
IL-C2-1-5000 (Socket contact)
Made by JAE (Japan) or equivalent

Unit: mm

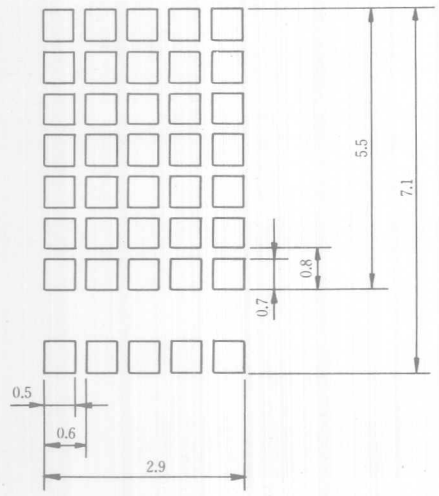


Fig. 1 Display pattern

Unit: mm

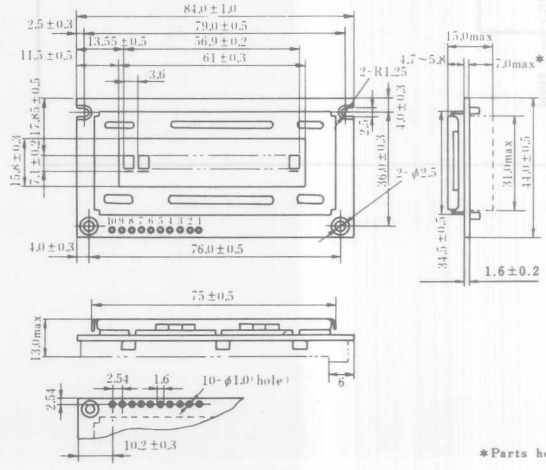


Fig. 2 External dimensions

HITACHI

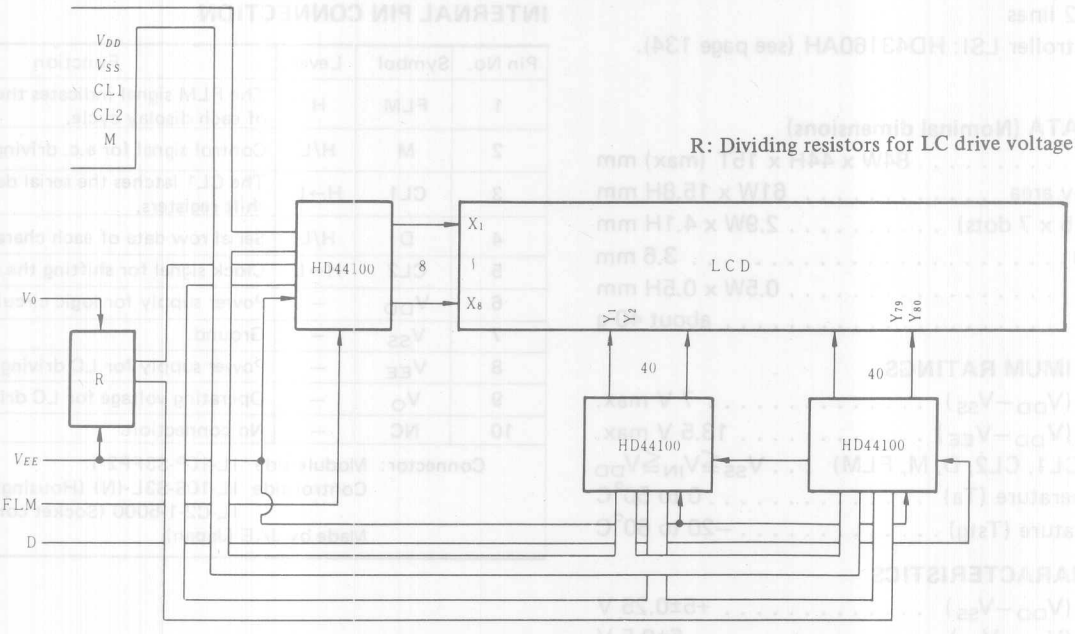


Fig. 3 Block diagram

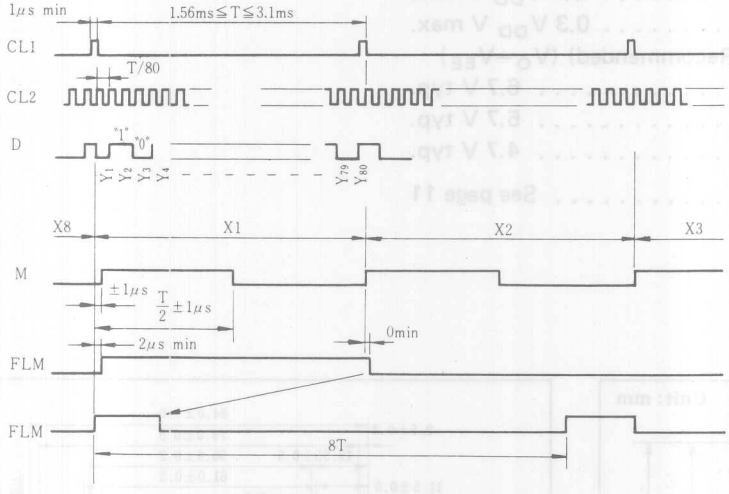
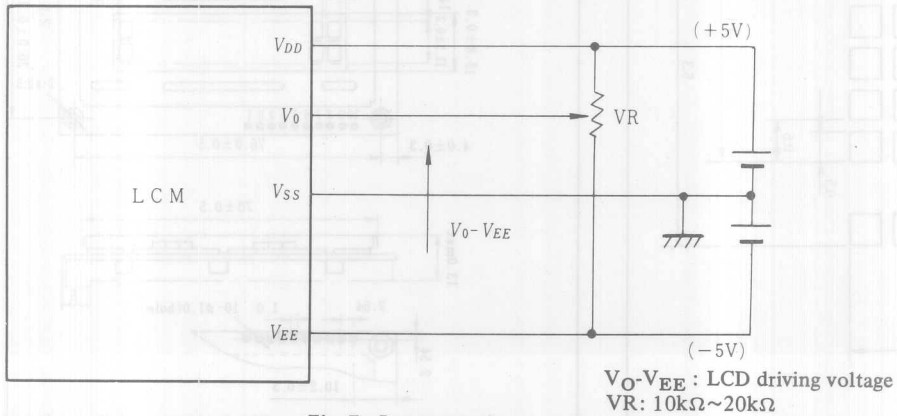


Fig. 4 Timing chart



V_O-V_{EE} : LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 5 Power supply

H2535

- 16 character x 2 lines
- Attachable controller LSI: HD43160AH (see page 134).

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 84W x 44H x 15T (max) mm
Effective display area . . . . . 61W x 15.8H mm
Character size (5 x 7 dots) . . . . . 2.9W x 4.1H mm
Character pitch . . . . . 3.6 mm
Dot size . . . . . 0.5W x 0.5H mm
Weight . . . . . about 40 g

ABSOLUTE MAXIMUM RATINGS

Supply voltage ($V_{DD}-V_{SS}$) . . . . . 7 V max.
($V_{DD}-V_{EE}$) . . . . . 13.5 V max.
Input voltage (CL1, CL2, D, M, FLM) . . . $V_{SS} \leqq V_{IN} \leqq V_{DD}$
Operating temperature (Ta) . . . . . 0 to 50°C
Storage temperature (Tstg) . . . . . −20 to 60°C

ELECTRICAL CHARACTERISTICS

Power supplies ($V_{DD}-V_{SS}$) . . . . . +5±0.25 V
($V_{EE}-V_{SS}$) . . . . . −5±0.5 V
Current consumption +5V . . . . . 1 mA max.
−5V . . . . . 1 mA max.
Input high voltage . . . . . 0.7 V_{DD} V min.
Input low voltage . . . . . 0.3 V_{DD} V max.
Power supply for LCD drive (Recommended) (V_O-V_{EE})
Ta = 0°C . . . . . 6.7 V typ.
Ta = 25°C . . . . . 5.7 V typ.
Ta = 50°C . . . . . 4.7 V typ.

OPTICAL DATA . . . . . See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	FLM	H	The FLM signal indicates the beginning of each display cycle.
2	M	H/L	Control signal for a.c. driving.
3	CL1	H→L	The CL1 latches the serial data in the shift registers.
4	D	H/L	Serial row data of each character.
5	CL2	H→L	Clock signal for shifting the serial data.
6	V_{DD}	–	Power supply for logic circuit.
7	V_{SS}	–	Ground.
8	V_{EE}	–	Power supply for LC driving.
9	V_O	–	Operating voltage for LC driving.
10	NC	–	No connection.

Connector: Module side IL-10P-S3FP2-1
Control side IL-10S-S3L-(N) (Housing)
IL-C2-1-5000 (Socket contact)
Made by JAE (Japan)

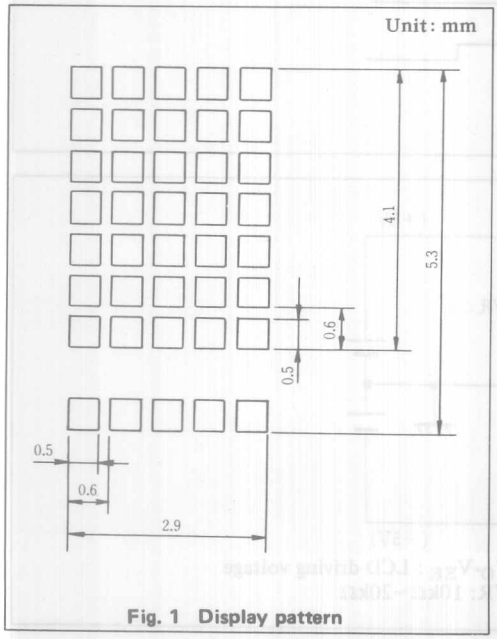


Fig. 1 Display pattern

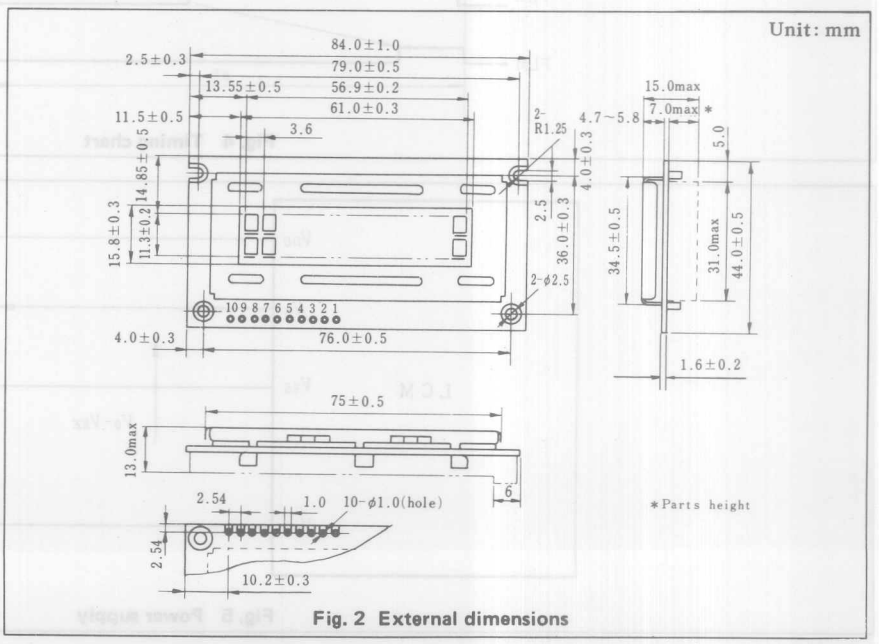


Fig. 2 External dimensions

HITACHI

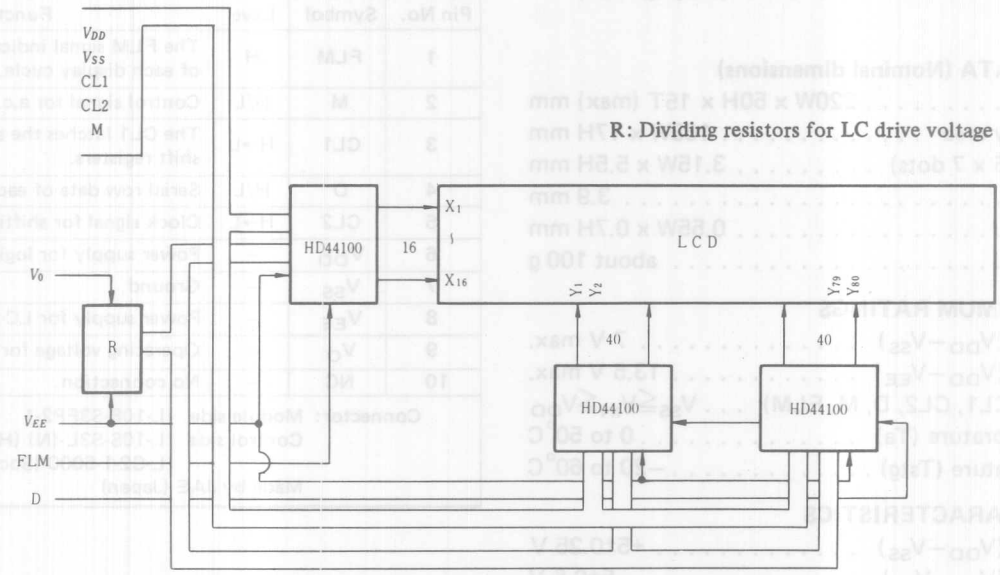


Fig. 3 Block diagram

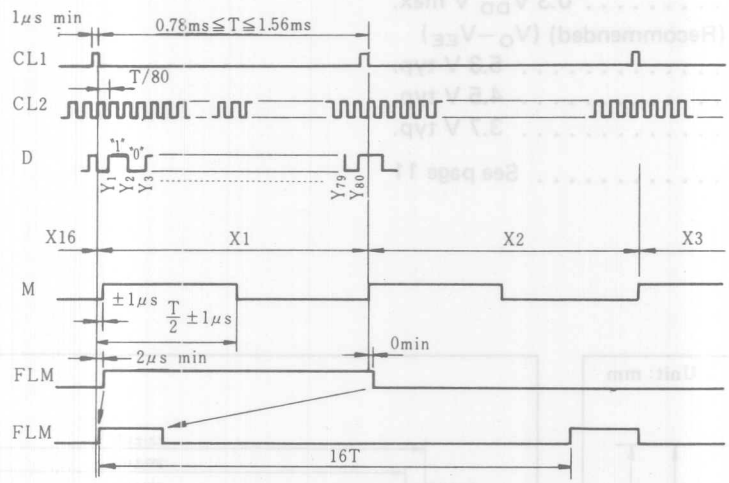
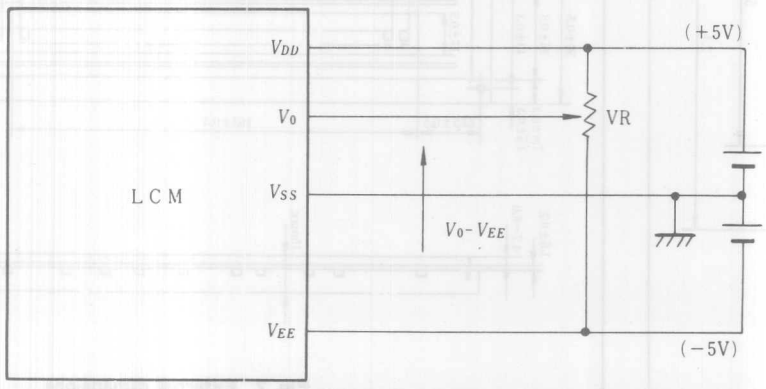


Fig. 4 Timing chart



V_O-V_{EE} : LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 5 Power supply

H2538A

- 40 character x 1 line
- Attachable controller LSI: HD43160AH (see page 134).

MECHANICAL DATA (Nominal dimensions)

Module size	220W x 50H x 15T (max) mm
Effective display area	163W x 17H mm
Character size (5 x 7 dots)	3.15W x 5.5H mm
Character pitch	3.9 mm
Dot size	0.55W x 0.7H mm
Weight	about 100 g

ABSOLUTE MAXIMUM RATINGS

Supply voltage ($V_{DD}-V_{SS}$)	7 V max.
($V_{DD}-V_{EE}$)	13.5 V max.
Input voltage (CL1, CL2, D, M, FLM)	$V_{SS} \leqq V_{IN} \leqq V_{DD}$
Operating temeprature (Ta)	0 to 50°C
Storage temperature (Tstg)	−20 to 60°C

ELECTRICAL CHARACTERISTICS

Power supplies ($V_{DD}-V_{SS}$)	+5±0.25 V
($V_{EE}-V_{SS}$)	−5±0.5 V
Current consumption +5V	1 mA max.
−5V	1 mA max.
Input high voltage	0.7 V_{DD} V min.
Input low voltage	0.3 V_{DD} V max.
Power supply for LCD drive (Recommended) (V_O-V_{EE})	
Ta = 0°C	5.3 V typ.
Ta = 25°C	4.5 V typ.
Ta = 50°C	3.7 V typ.

OPTICAL DATA ..... See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	FLM	H	The FLM signal indicates the beginning of each display cycle.
2	M	H/L	Control signal for a.c. driving.
3	CL1	H→L	The CL1 latches the serial data in the shift registers.
4	D	H/L	Serial row data of each character.
5	CL2	H→L	Clock signal for shifting the serial data.
6	V_{DD}	–	Power supply for logic circuit.
7	V_{SS}	–	Ground.
8	V_{EE}	–	Power supply for LC driving.
9	V_O	–	Operating voltage for LC driving.
10	NC	–	No connection.

Connector: Module side IL-10P-S3FP2-1
Control side IL-10S-S3L-(N) (Housing)
IL-C2-1-5000 (Socket contact)
Made by JAE (Japan)

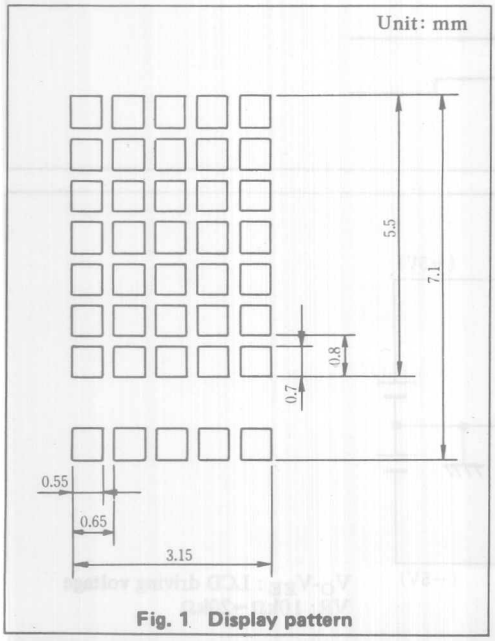


Fig. 1 Display pattern

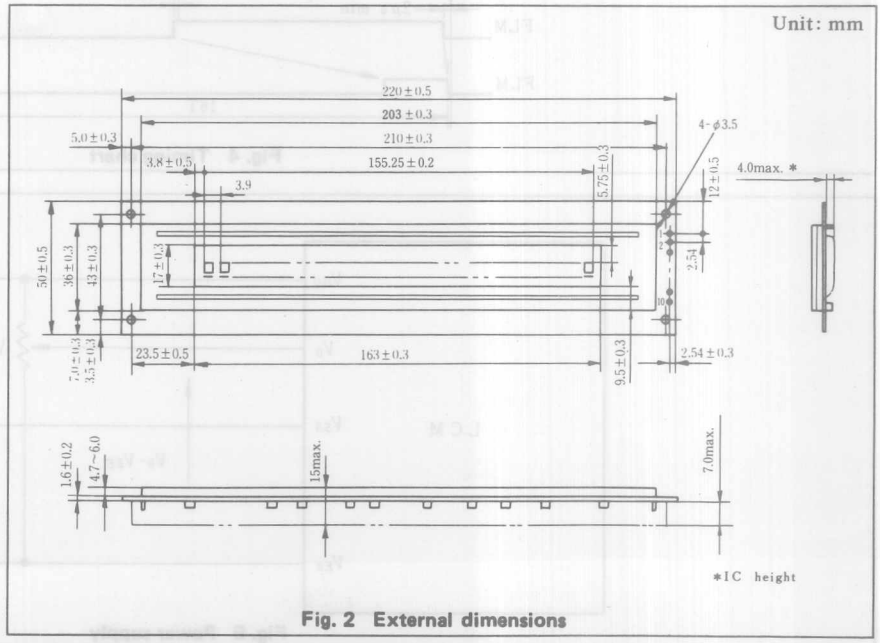
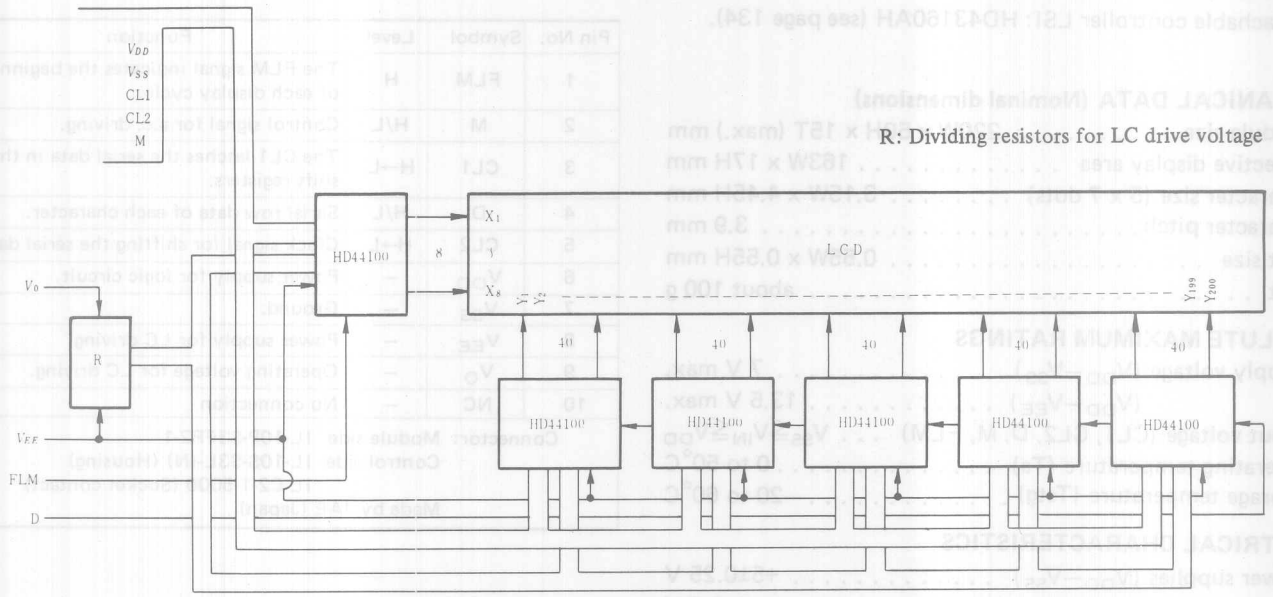


Fig. 2 External dimensions

HITACHI



R: Dividing resistors for LC drive voltage

Fig. 3 Block diagram

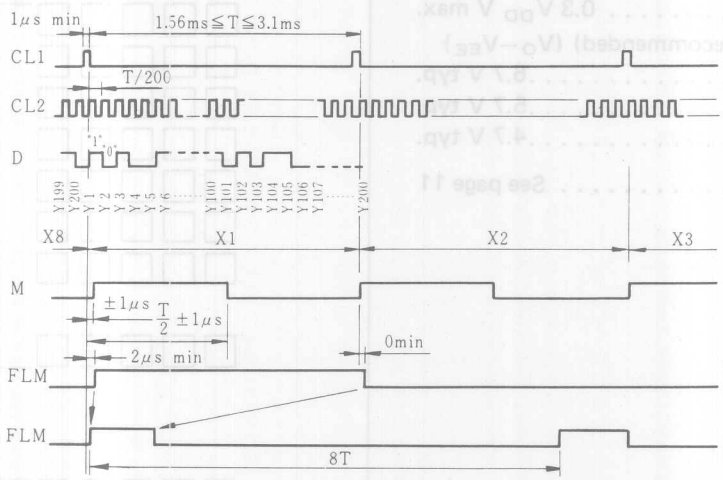
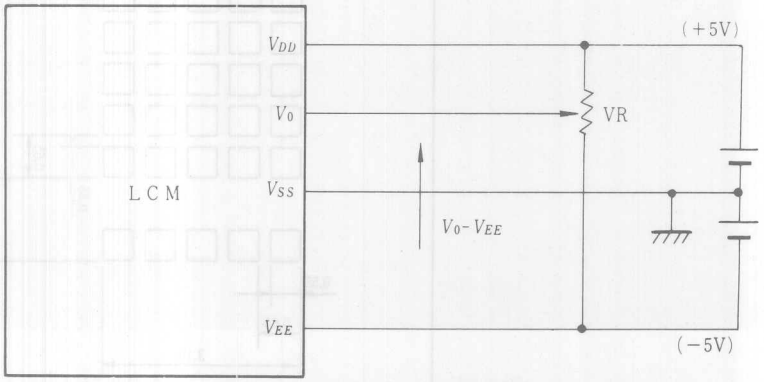


Fig. 4 Timing chart



V_O-V_{EE}: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 5 Power supply

H2539

- 40 character x 2 lines
- Attachable controller LSI: HD43160AH (see page 134).

MECHANICAL DATA (Nominal dimensions)

Module size	220W x 50H x 15T (max.) mm
Effective display area	163W x 17H mm
Character size (5 x 7 dots)	3.15W x 4.45H mm
Character pitch	3.9 mm
Dot size	0.55W x 0.55H mm
Weight	about 100 g

ABSOLUTE MAXIMUM RATINGS

Supply voltage ($V_{DD}-V_{SS}$)	7 V max.
($V_{DD}-V_{EE}$)	13.5 V max.
Input voltage (CL1, CL2, D, M, FLM)	$V_{SS} \leqq V_{IN} \leqq V_{DD}$
Operating temperature (Ta)	0 to 50°C
Storage temperature (Tstg)	−20 to 60°C

ELECTRICAL CHARACTERISTICS

Power supplies ($V_{DD}-V_{SS}$)	+5±0.25 V
($V_{EE}-V_{SS}$)	−5±0.5 V
Current consumption +5V	1 mA max.
−5V	1 mA max.
Input high voltage	0.7 V_{DD} V min.
Input low voltage	0.3 V_{DD} V max.
Power supply for LCD drive (Recommended) (V_O-V_{EE})	
Ta = 0°C	6.7 V typ.
Ta = 25°C	5.7 V typ.
Ta = 50°C	4.7 V typ.

OPTICAL DATA ..... See page 11

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	FLM	H	The FLM signal indicates the beginning of each display cycle.
2	M	H/L	Control signal for a.c. driving.
3	CL1	H→L	The CL1 latches the serial data in the shift registers.
4	D	H/L	Serial row data of each character.
5	CL2	H→L	Clock signal for shifting the serial data.
6	V_{DD}	–	Power supply for logic circuit.
7	V_{SS}	–	Ground.
8	V_{EE}	–	Power supply for LC driving.
9	V_O	–	Operating voltage for LC driving.
10	NC	–	No connection

Connector: Module side IL-10P-S3FP2-1
Control side IL-10S-S3L-(N) (Housing)
IL-C2-1-5000 (Socket contact)
Made by JAE (Japan)

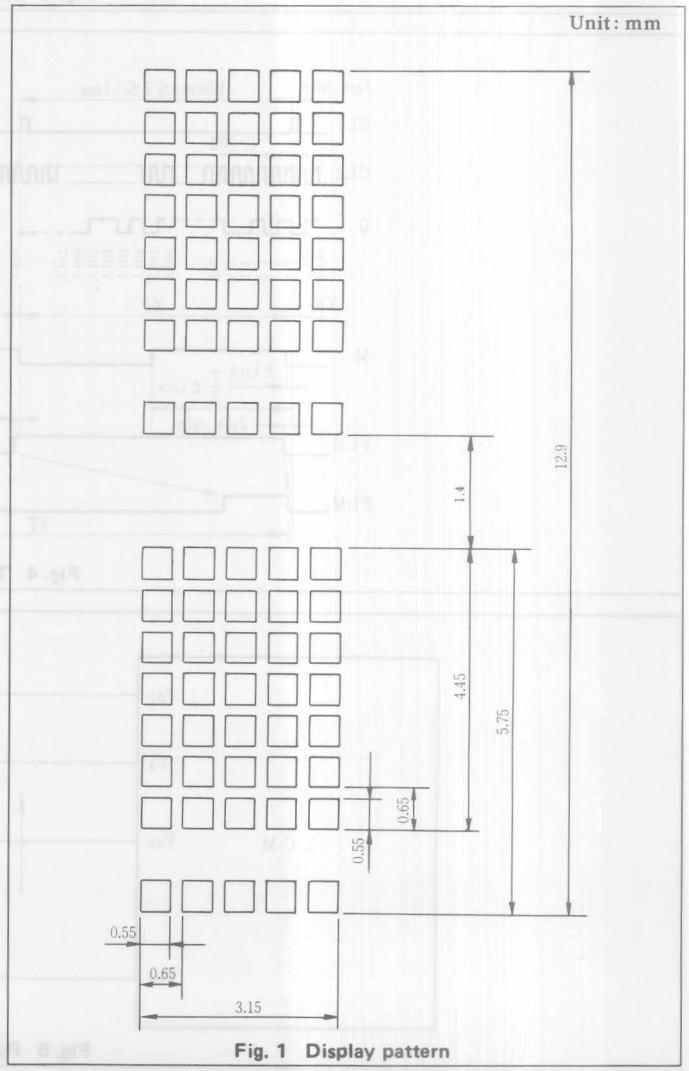


Fig. 1 Display pattern

Unit: mm

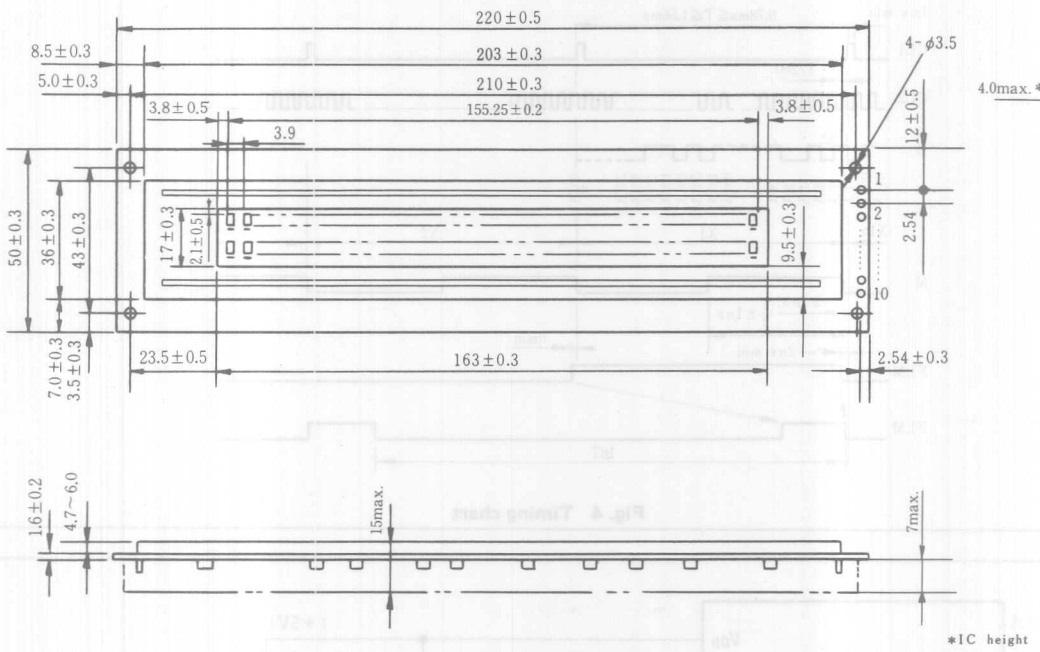
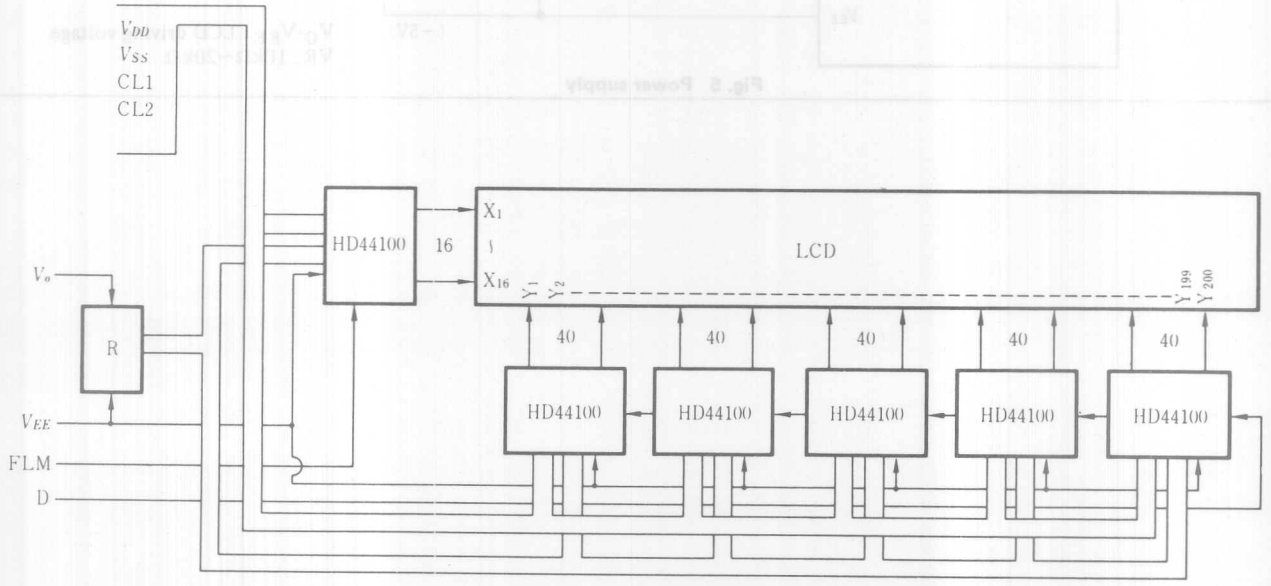


Fig. 2 External dimensions



R: Dividing resistors for LC drive voltage.

Fig. 3 Block diagram

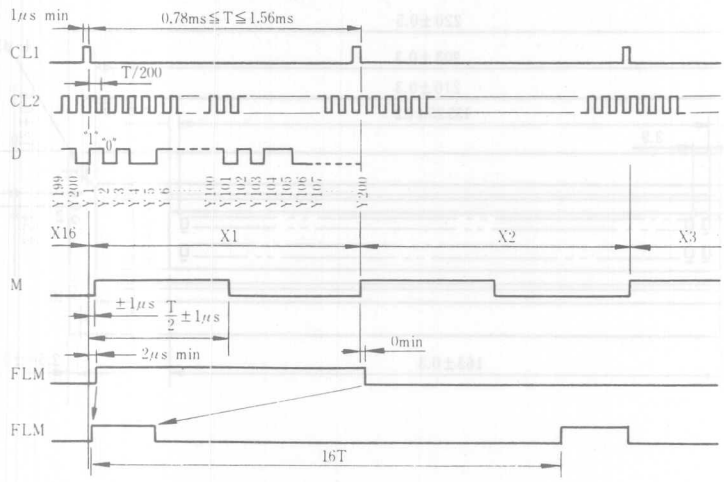
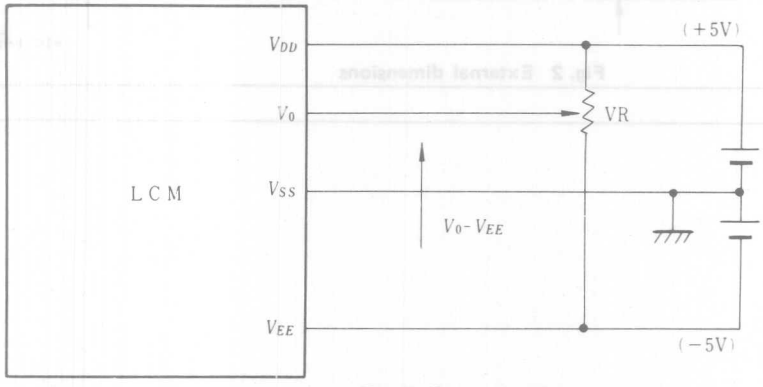


Fig. 4 Timing chart



V_O-V_{EE}: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 5 Power supply

SEGMENT TYPE LCD MODULE

This is a segment type LCD module containing the controller LSI for numerical display.

LM039

LM039

- 7 segment x 16 digits
- Controller LSI μPD7225G is built-in
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 87.0W x 27.5H x 11.0T (max.) mm
Effective display area . . . . . 64.7W x 13.3H mm
Character size . . . . . 2.2W x 6.4H mm
Character pitch . . . . . 3.9 mm

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V
Input "high" voltage (V_{IH}) . . . . . 0.7 V_{DD} V min.
Input "low" voltage (V_{IL}) . . . . . 0.3 V_{DD} V max.
Output "high" voltage (V_{OH})
($-I_{OH}$ = 10 μA) . . . . . V_{DD} − 0.5 V min.
Output "low" voltage (V_{OL})
(I_{OL} = 100 μA) . . . . . 0.5 V max.
Power supply current (I_{DD})
(V_{DD} = 5.0 V) . . . . . 0.21 mA typ.
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Du = 1/4

Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/4
Ta = 0°C . . . . . 3.32 V typ.
Ta = 25°C . . . . . 3.15 V typ.
Ta = 50°C . . . . . 2.70 V typ.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	V_{DD}	Power supply positive (5V)
3	V_0	LCD driving voltage
4	$\overline{SCK}$	Serial clock input
5	SI	Serial input
6	$\overline{CS}$	Chip select input
7	$\overline{BUSY}$	Busy output
8	C/$\overline{D}$	Command/Data select
9	$\overline{RESET}$	Reset input
10	NC	No connection

Unit: mm

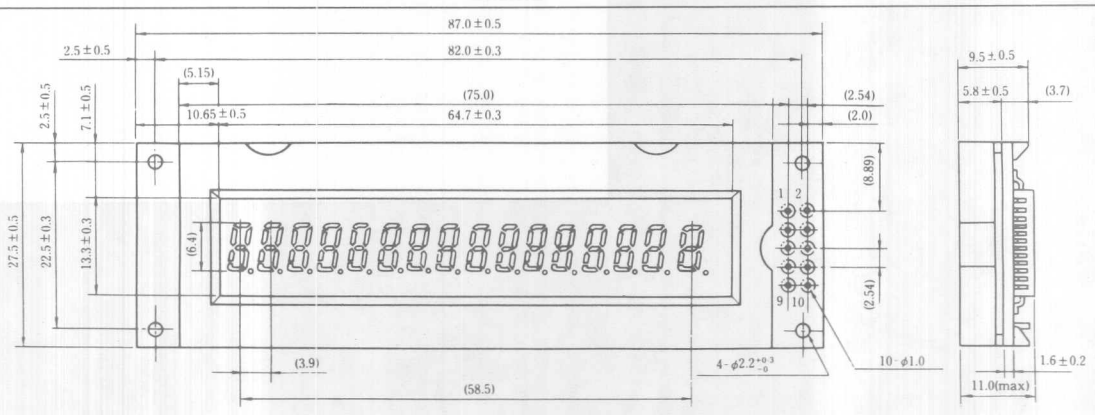


Fig. 1 External dimension

Unit: mm

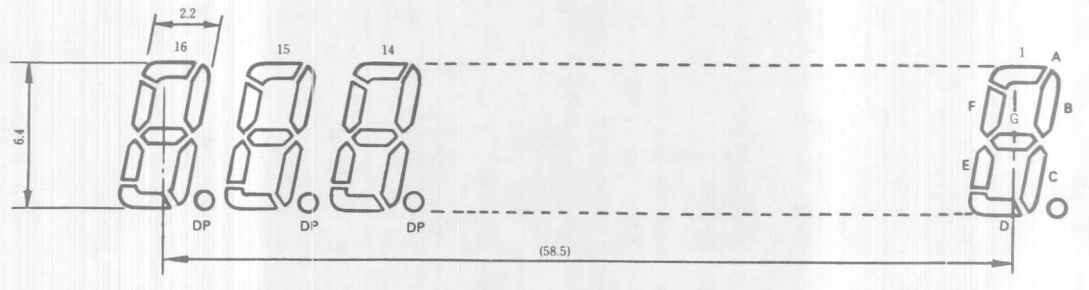
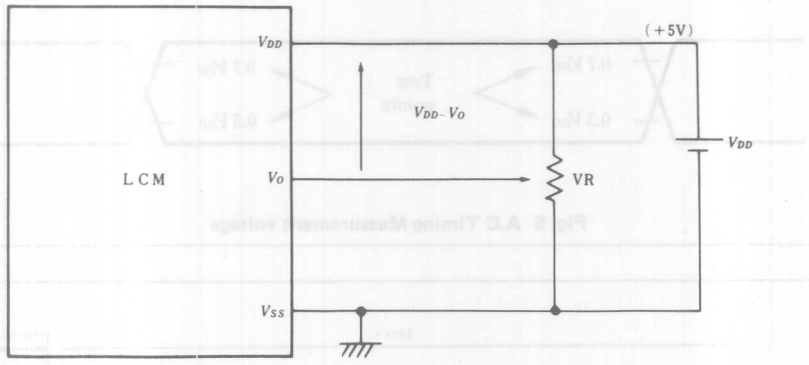


Fig. 2 Display pattern

HITACHI



$V_{DD} - V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

Fig. 3 Power supply

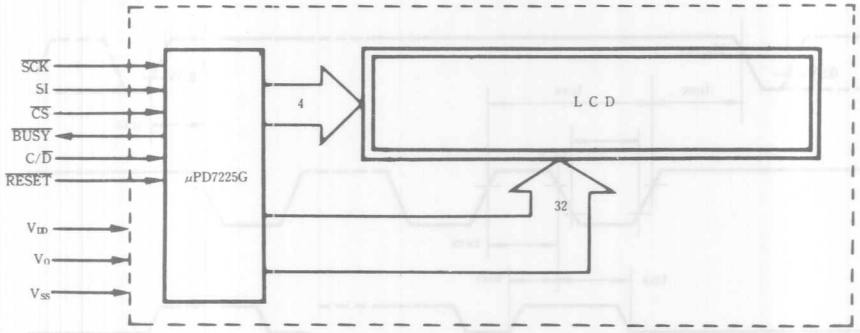


Fig. 4 Block diagram

INTERFACE TIMING

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle	t_{CYK}		900			ns
$\overline{SCK}$ pulse width high	t_{WHK}		400			ns
$\overline{SCK}$ pulse width low	t_{WLK}		400			ns
$\overline{BUSY}$ ↓ → $\overline{SCK}$ ↓ hold time	t_{HBK}		0			ns
SI setup time to $\overline{SCK}$ ↑	t_{SIK}		100			ns
SI hold time after $\overline{SCK}$ ↑	t_{HKI}		200			ns
8th $\overline{SCK}$ ↑ → $\overline{BUSY}$ ↓ delay time	t_{DKB}	CL = 50pF			3	μs
$\overline{CS}$ ↓ → $\overline{BUSY}$ ↓ delay time	t_{DCSB}	CL = 50pF			1.5	μs
C/$\overline{D}$ setup time to 8th $\overline{SCK}$ ↑	t_{SDK}		9			μs
C/$\overline{D}$ hold time after 8th $\overline{SCK}$ ↑	t_{HKD}		1			μs
$\overline{CS}$ hold time after 8th $\overline{SCK}$ ↑	t_{HKCS}		1			μs
$\overline{CS}$ pulse width high	t_{WHCS}		40			μs
$\overline{CS}$ pulse width low	t_{WLCS}		40			μs

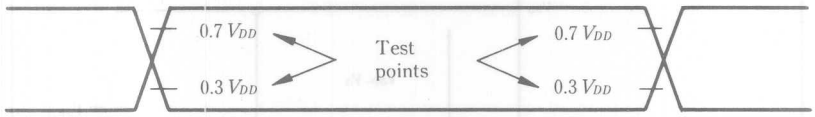


Fig. 5 A.C Timing Measurement voltage

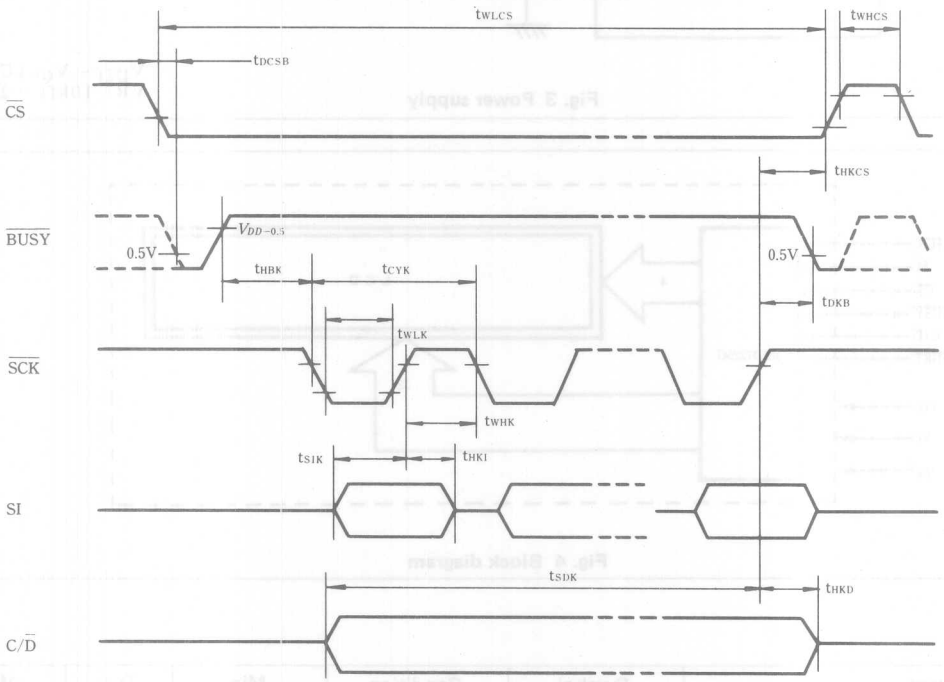


Fig. 6 Timing waveforms

Note : Power on sequence

(1) Power supply voltage should be applied to LCD module as figure 7.

(2) Input signals should not be applied to LCD module before power supply voltage is applied and reaches to specified voltage (5V ±0.5V).

If above sequence is not kept, C-MOS LSIs of LCD modules may be damaged due to latch up problem.

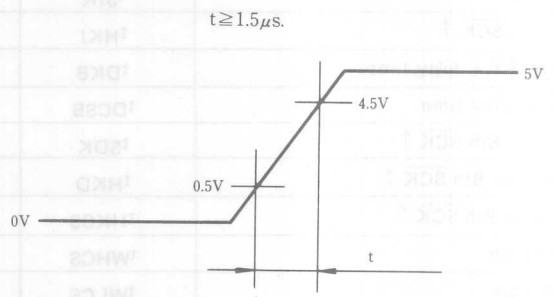


Fig. 7 Power supply voltage

DEOODED DISPLAY RAM DATA

Display byte (HEX)	Character	4-backplane multiplex Display RAM address N+1	N
0 0	0.	D	7
0 1	1.	O	6
0 2	2.	E	3
0 3	3.	A	7
0 4	4.	3	6
0 5	5.	B	5
0 6	6.	F	5
0 7	7.	O	7

Display byte (HEX)	Character	4-backplane multiplex Display RAM address N+1	N
0 8	8.	F	7
0 9	9.	F	7
0 A	A.	2	0
0 B	b.	F	1
0 C	C.	D	1
0 D	d.	A	0
0 E	E.	E	4
0 F	F.	O	0

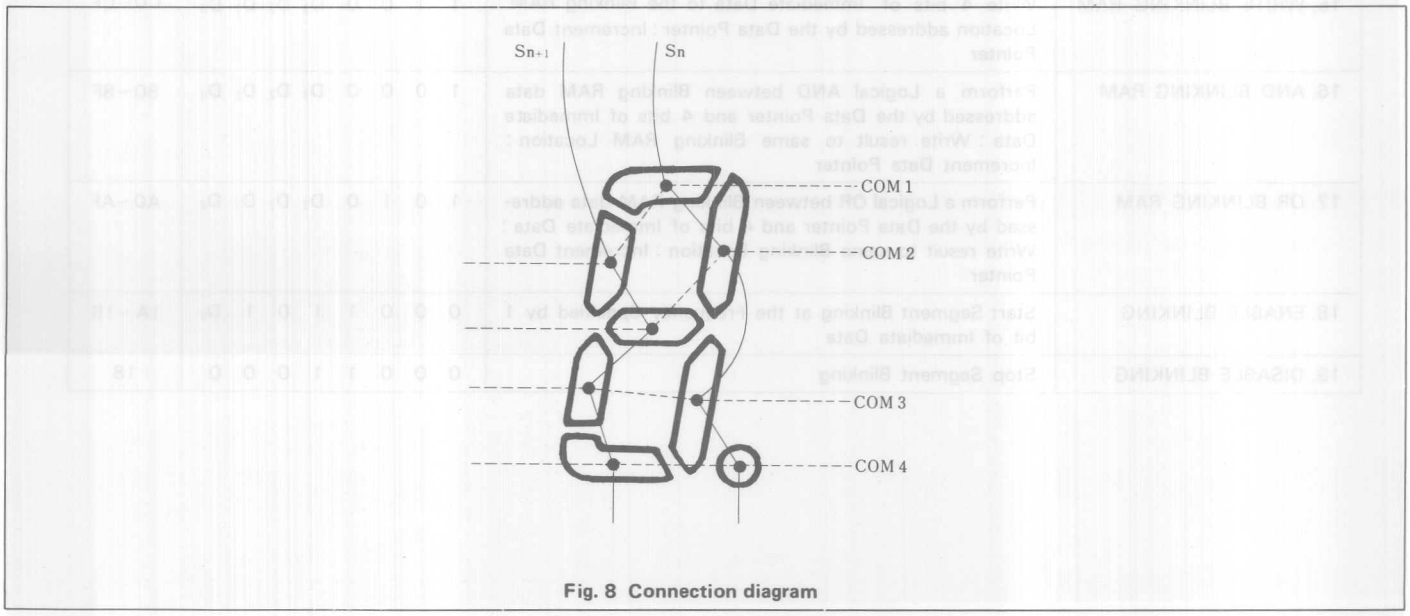


Fig. 8 Connection diagram

COMMAND

Command	Description	Instruction code								
		Binary								HEX
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1. MODE SET	Initialize the μPD7225 1) LCD Drive Configuration 2) LCD Bias Voltage Configuration 3) LCD Frame Frequency	0	1	0	0	0	0	1	0	42
2.UNSYNCHRONOUS DATA TRANSFER	Synchronize Display RAM data transfer to Display Latch with CS	0	0	1	1	0	0	0	0	30
3. SYNCHRONOUS DATA TRANSFER	Synchronize Display RAM data transfer to Display Latch with LCD Drive Cycle	0	0	1	1	0	0	0	1	31
4. INTERRUPT DATA TRANSFER	Interrupt Display RAM data transfer to Display Latch	0	0	1	1	1	0	0	0	38
5. LOAD DATA POINTER	Load Data Pointer with 5 bits of Immediate Data	1	1	1	D_4	D_3	D_2	D_1	D_0	EO~FF
6. CLEAR DISPLAY RAM	Clear the Display RAM and reset the Data Pointer	0	0	1	0	0	0	0	0	20
7. WRITE DISPLAY RAM	Write 4 bits of Immeditae Data to the Display RAM Location addressed by the Data Pointer : Increment Data Pointer	1	1	0	1	D_3	D_2	D_1	D_0	DO~DF
8. AND DISPLAY RAM	Perform a Logical AND between the Display RAM data addressed by the Data Pointer and 4 bits of Immediate Data : Write result to same Display RAM Location. Increment Data Pointer	1	0	0	1	D_3	D_2	D_1	D_0	90~9F
9. OR DISPLAY RAM	Perform a Logical OR between the Display RAM data addressed by the Data Pointer and 4 bits of Immediate Data : Write result to same Display RAM Location : Increment Data Pointer	1	0	1	1	D_3	D_2	D_1	D_0	BO~BF
10. ENABLE SEGMENT DECODER	Start use of the Segment Decoder	0	0	0	1	0	1	0	1	15
11. DISABLE SEGMENT DECODER	Stop use of the Segment Decoder	0	0	0	1	0	1	0	0	14
12. ENABLE DISPLAY	Turn on the LCD	0	0	0	1	0	0	0	1	11
13. DISABLE DISPLAY	Turn off the LCD	0	0	0	1	0	0	0	0	10
14. CLEAR BLINKING RAM	Clear the Blinking RAM and reset the Data Pointer	0	0	0	0	0	0	0	0	00
15. WRITE BLINKING RAM	Write 4 bits of Immediate Data to the Blinking RAM Location addressed by the Data Pointer : Increment Data Pointer	1	1	0	0	D_3	D_2	D_1	D_0	CO~CF
16. AND BLINKING RAM	Perform a Logical AND between Blinking RAM data addressed by the Data Pointer and 4 bits of Immediate Data : Write result to same Blinking RAM Location : Increment Data Pointer	1	0	0	0	D_3	D_2	D_1	D_0	80~8F
17. OR BLINKING RAM	Perform a Logical OR between Blinking RAM data addressed by the Data Pointer and 4 bits of Immediate Data : Write resuit to same Blinking Location : Increment Data Pointer	1	0	1	0	D_3	D_2	D_1	D_0	AO~AF
18. ENABLE BLINKING	Start Segment Blinking at the Frequency Specified by 1 bit of Immediata Data	0	0	0	1	1	0	1	D_0	1A~1B
19. DISABLE BLINKING	Stop Segment Blinking	0	0	0	1	1	0	0	0	18

HOW TO USE HITACHI'S BUILT-IN CONTROLLER DRIVER LCD-II (HD44780) DOT MATRIX LCD MODULE

Note: Refer to the following for details of HD44780 (LCD-II)
Hitachi, Ltd.
Semiconductor & Integrated Circuits Div.
New Marunouchi Bldg., 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo, 100 Tel: 03-212-1111

■ INTRODUCTION

The LCD-II (HD44780) is a dot matrix liquid crystal display controller & driver LSI that displays alphanumerics, kana characters and symbols. It drives dot matrix liquid crystal display under 4-bit or 8-bit microcomputer or microprocessor control. All the functions required for dot matrix liquid crystal display drive are internally provided on one chip.

The user can complete dot matrix liquid crystal display systems with less number of chips by using the LCD-II (HD44780). If a driver LSI HD44100H is externally connected to the HD44780, up to 80 characters can be displayed.

The LCD-II is produced in the CMOS process. Therefore, the combination of the LCD-II with a CMOS microcomputer or microprocessor can accomplish a portable battery-drive device with lower power dissipation.

■ FEATURES

- Capable of interfacing to 4-bit or 8-bit MPU.
- Display data RAM . . . . . 80 x 8 bits
  (80 characters, max.)
- Character generator ROM . . . .
  Character font 5 x 7 dots: 160 characters
  Character font 5 x 10 dots: 32 characters
- Both display data and character generator RAMs can be read from the MPU.
- Wide range of instruction functions
  Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF, Display character blink, Cursor shift, Display shift
- Internal automatic reset circuit at power ON. (Internal reset circuit)

1. Applicable type

(1) 1 line series
LM054·H2570·LM015·LM568AF·LM020L·LM070L·
LM038·LM027·H2571·H2572·LM058

(2) 2 line series
LM052L·LM016L·LM032L·LM060L·LM017L·LM018L

(3) 4 line series
LM041L·LM044L

2. Connecting MPU with LCM

2.1 Driver circuit block diagram

Figure 1 shows the driver circuit block diagram of LCM with built-in controller LSI. Controller LSI HD44780 (LCD-II) is built-in this LCM. Also extended LCD driver LSI is built in the LCM that displays more than 16 digits.

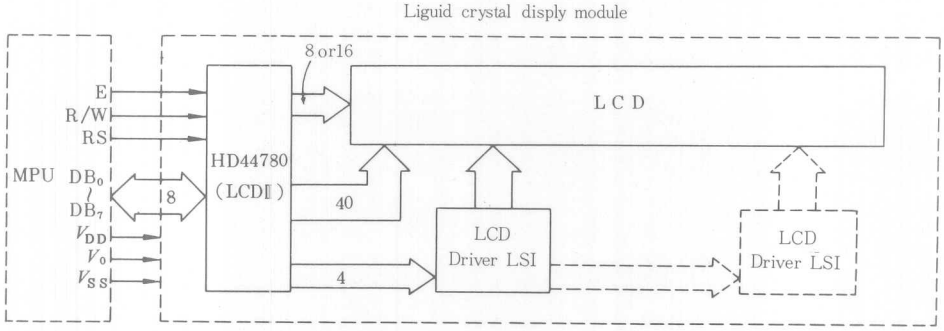


Fig. 1 Driver circuit block diagram

2.2 Interfacing to MPU

In the HD44780, data can be sent in either 4-bit 2-operation or 8-bit 1-operation so it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4-bits long, data is transferred using only 4 buses: $DB_4 \sim DB_7$. $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first, then the lower order 4 bits (content of $DB_0 \sim DB_3$ when interface data is 8 bits long) is transferred. Check the busy flag after 4-bit data has been transferred twice (one instruction). A 4-bit 2-operation will then transfer the busy flag and address counter data.

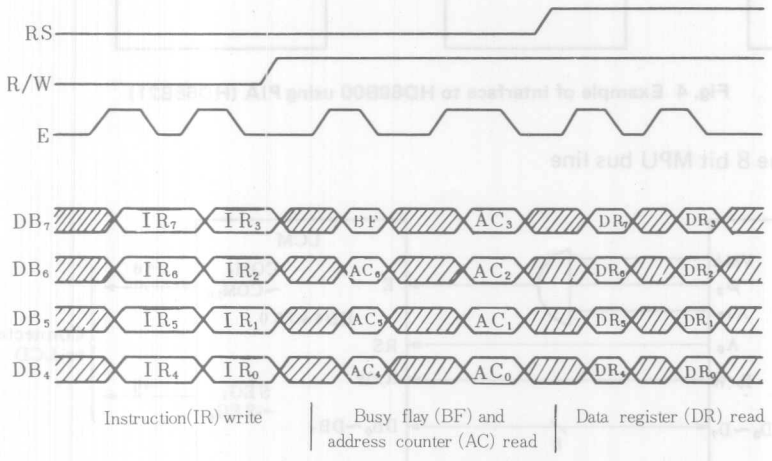


Fig. 2 4-bit data transfer example

(2) When interface data is 8 bit long, data is transferred using the 8 data buses of $DB_0 \sim DB_7$.

2.3 Interface to MPU

(1) Interface to 8-bit MPU

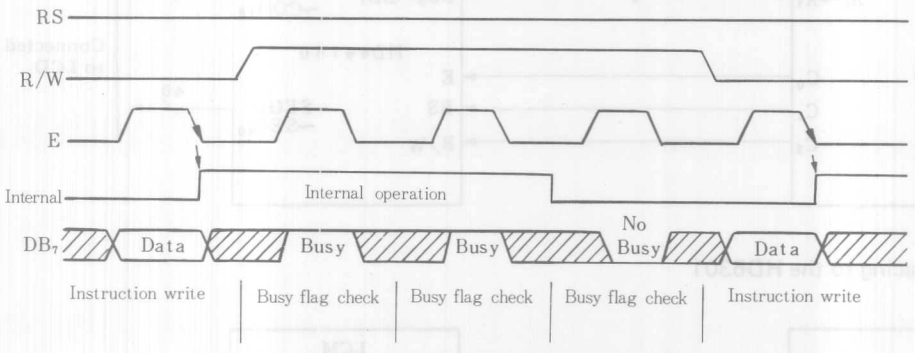


Fig. 3 Example of busy flag check timing sequence

① When connecting to 8-bit MPU through PIA

Fig. 4 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/W and RS respectively. Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

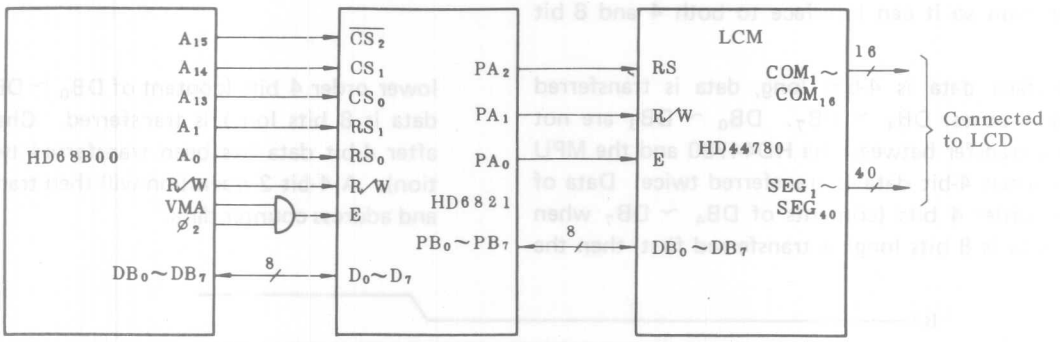
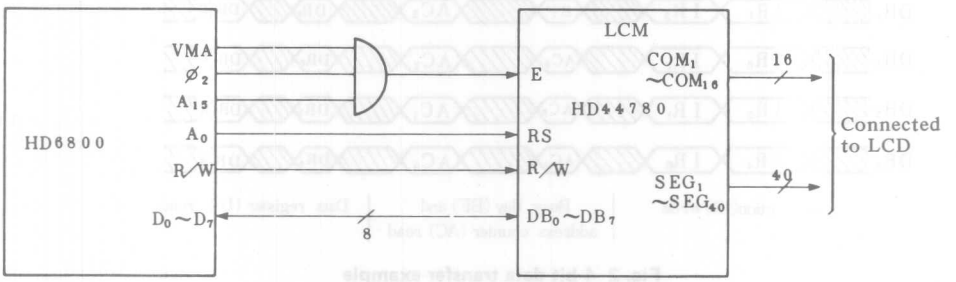
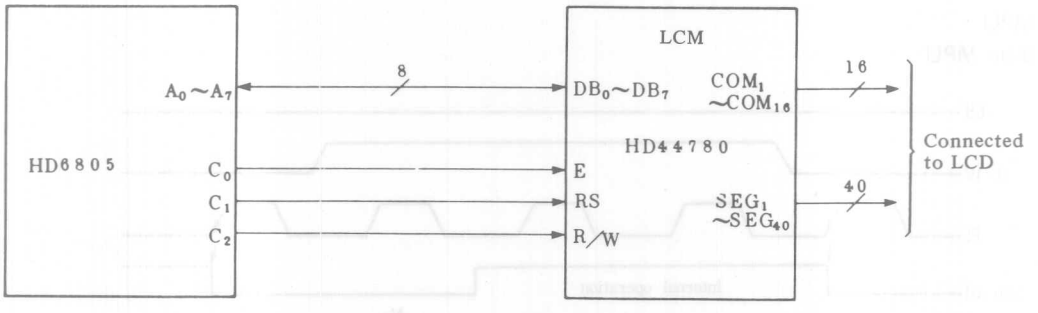


Fig. 4 Example of interface to HD68B00 using PIA (HD68B21)

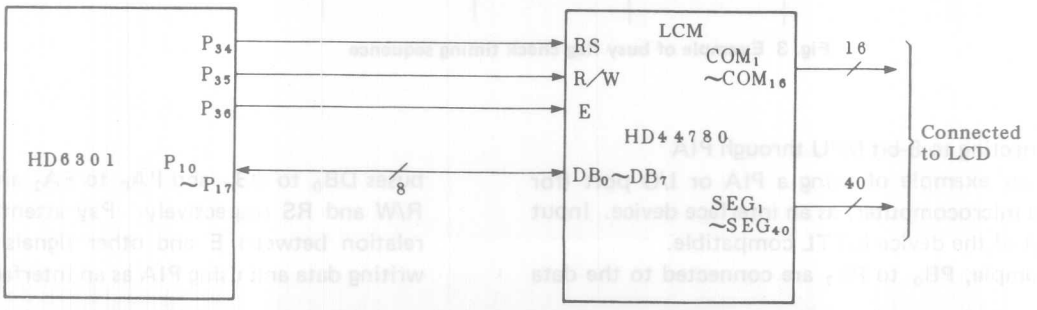
② Connecting directly to the 8 bit MPU bus line



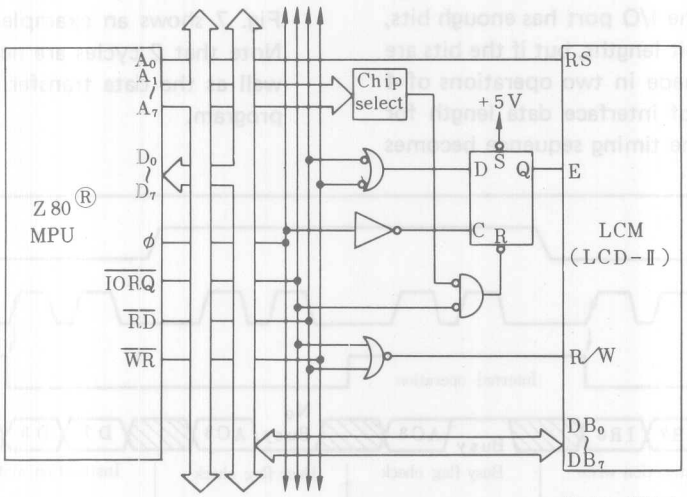
③ Example of interfacing to the HD6805



④ Example of interfacing to the HD6301



⑤ Example of interfacing to Z80 MPU



Note: 280 is the trademark of ZILOG, U.S.A.

(a) Above circuit is an example of connection with Z80 MPU and HD44780A00 as an I/O equipment. It can be used as a part of memories by using MREQ signal.

(b) A0 signal can be used for RS signal.
A0 = 0: Instruction register is selected.
A0 = 1: Data register is selected.

(c) In order to check busy flag, transfer the data of $DB_0 \sim DB_7$ to A register (accumulator) by executing In/Out instruction. After that, busy flag can be easily checked by examining DB_7.

⑥ Example of interfacing to 80 CPU family

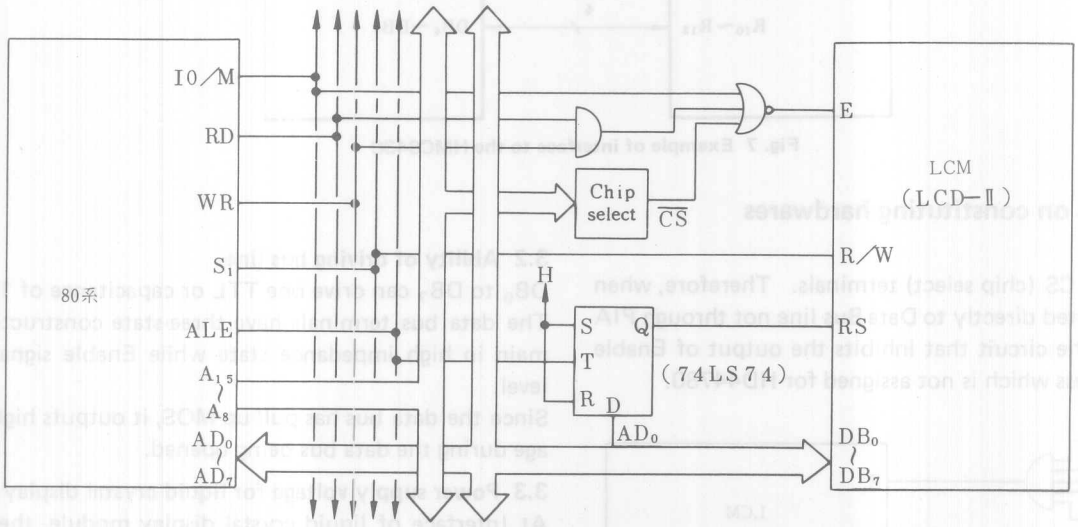


Fig. 5 Example of connection with LCM being used as a part of memories on the determined address.

Figure 5 is an example of connection with LCD module being used as a part of memories on the determined address.

Generates RS signal (Register Select signal) by latching the content of AD_0 at the rising edge of ALE signal. By using this method, you can obtain RS signal from the AD_0 among 8 bit addresses generated at the clock of the first machine cycle. In case of using LCD module as an I/O equipment, chip select signal is necessarily activated when IO/M signal is "High" level.

Furthermore, by using A8 for RS signal, the interface is easily realized.

By both methods, busy flag can be checked by storing status data into A register (Accumulator) and examining the bit 7 by software.

(2) Interface to 4-bit MPU

The HD44780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex. (See Fig. 6)

Fig. 7 shows an example of interface to the HMCS43C. Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.

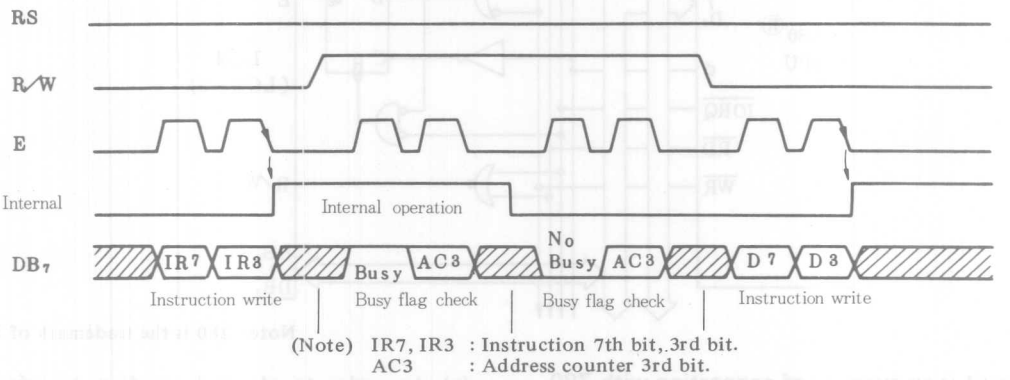


Fig. 6 An example of 4 bit data transfer timing sequence

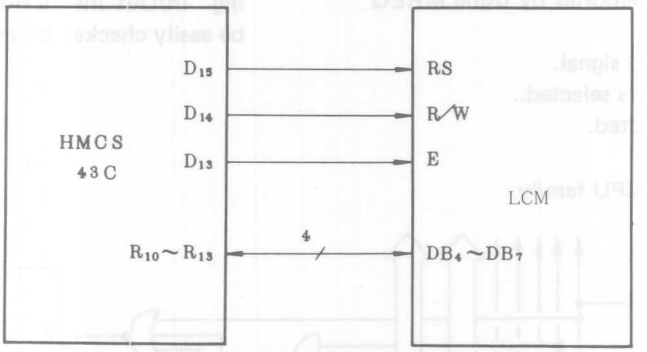


Fig. 7 Example of interface to the HMCS43C

3. Precautions on constituting hardwares

3.1 Chip select

HD44780 has no CS (chip select) terminals. Therefore, when this LSI is connected directly to Data Bus line not through PIA and so on, add the circuit that inhibits the output of Enable signal at the address which is not assigned for HD44780.

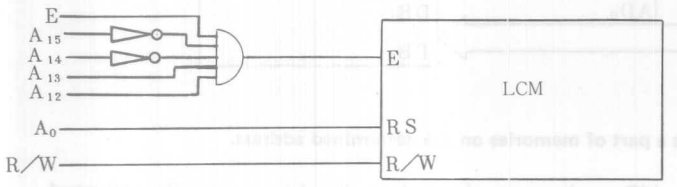


Fig. 8 Example of addresses $(3000)_{16}$ ~ $(3FFF)_{16}$ being assigned for HD44780

3.2 Ability of driving bus line

DB_0 to DB_7 can drive one TTL or capacitance of 130 pF.

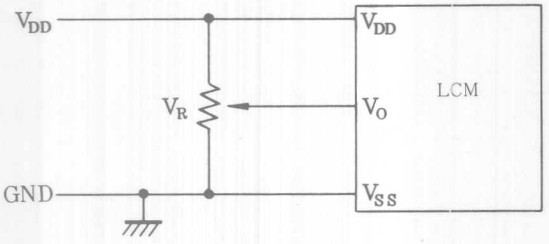
The data bus terminals have three-state constructions and remain in high impedance state while Enable signal being low level.

Since the data bus has pull up MOS, it outputs high level voltage during the data bus being opened.

3.3 Power supply voltage for liquid crystal display drive

At Interface of liquid crystal display module, there are three power supply terminals, V_{DD}, GND, and V_0. LCD module is driven by the voltage that is equal to $V_{DD} - V_0$, when supplying power for liquid crystal display drive to V_0 terminal. Since suitable voltage of power supply for LCD shifts according to temperature change adjust supplying power to LCD by referring to Fig. 9 or Fig. 10.

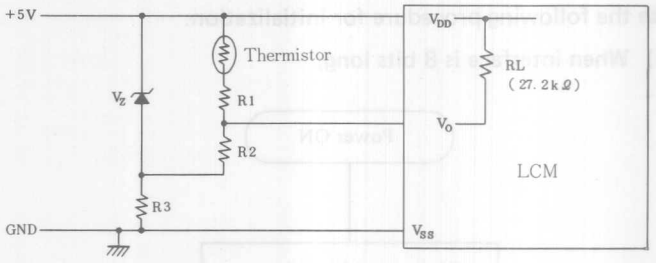
(1) Example of variable driving voltage by a variable resistance (VR)
The driving voltage can be changed by VR to compensate the influence of surrounding temperature.



Recommended V_R value=10kΩ ~ 20kΩ

Fig. 9 Variable driving voltage circuit

(2) Example of a thermal compensator circuit
When setting the voltage, refer to Table-1



Thermistor { RT=15kΩ (Ta=25°C)
B=4300

Fig. 10 Example of a thermal compensator circuit

Table 1

LCD module	Duty	Recommended driving voltage		Typical circuit parameter			
		Ta(°C)	$V_{DD}-V_O$(V)	V_Z(V)	R1(kΩ)	R2(kΩ)	R3(kΩ)
LM015 LM027 LM038 LM054	1/8	0	4.0	4.5	2.2	2.8	1.0
		25	3.7				
		50	3.3				
LM058 H2570 H2571 H2572	1/11	0	4.3	4.5	2.2	3.2	0.3
		25	3.9				
		50	3.3				
LM032L	1/16	0	4.6	5.0	0.1	1.3	0.1
		25	4.4				
		50	4.2				

4. Initialization

4.1 Initializing by internal reset circuit

The HD44780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. (BF = 1) The busy state is 10 ms after V_{CC} rises to 4.5 V.

(1) Display clear
(2) Function set ..... DL = 1 : 8 bit long interface data
N = 0 : 1-line display
F = 0 : 5 x 7 dot character font
(3) Display ON/OFF control ..... D = 0 : Display OFF
C = 0 : Cursor OFF
B = 0 : Blink OFF
(4) Entry mode set .... I/D = 1 : +1 (increment)
S = 0 : No shift
(5) Write DD RAM

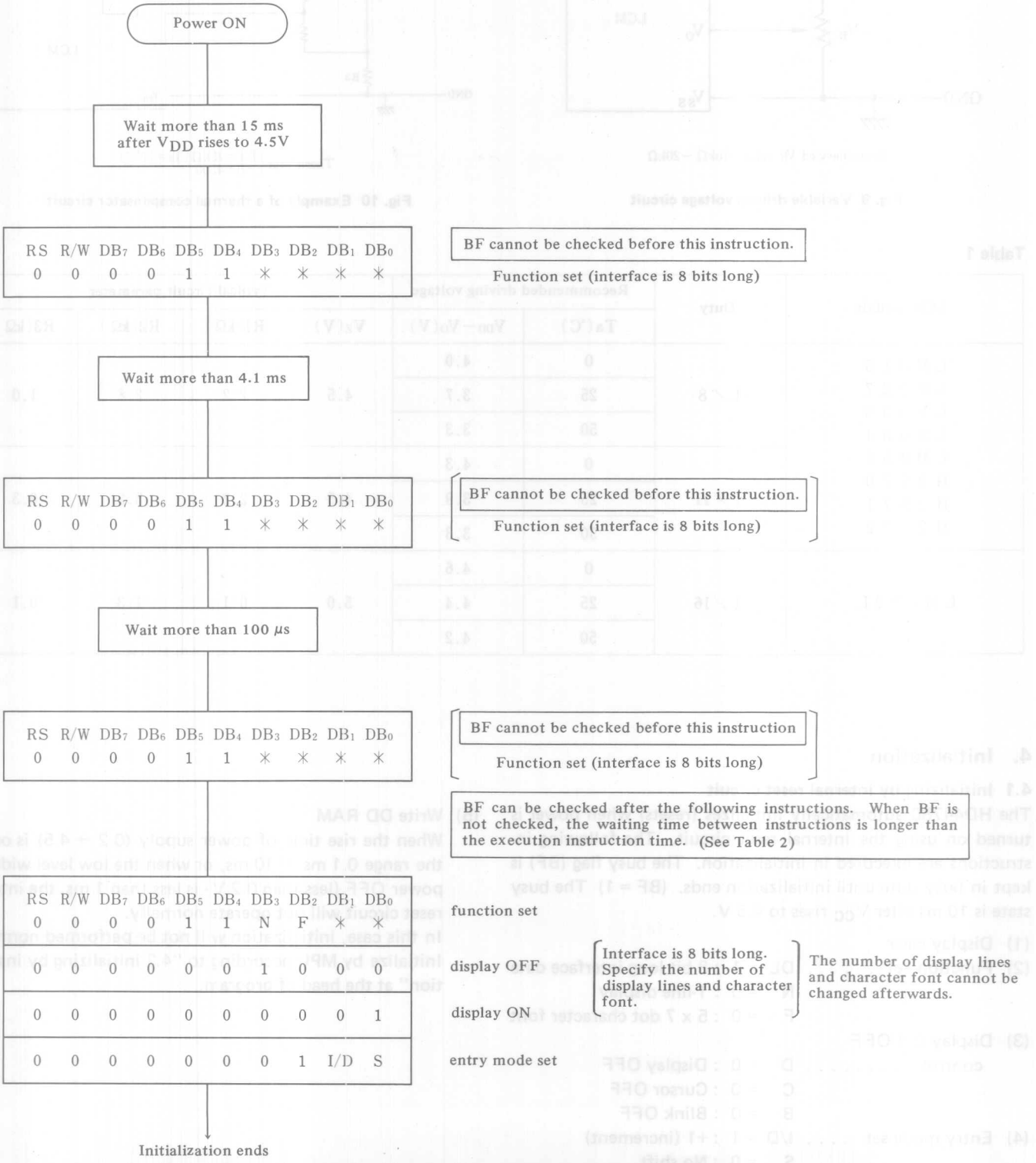
When the rise time of power supply (0.2 → 4.5) is out of the range 0.1 ms ~ 10 ms, or when the low level width of power OFF (less than 0.2 V) is less than 1 ms, the internal reset circuit will not operate normally.
In this case, initialization will not be performed normally. Initialize by MPU according to "4.2 initializing by instruction" at the head of program.

4.2 Initializing by instruction

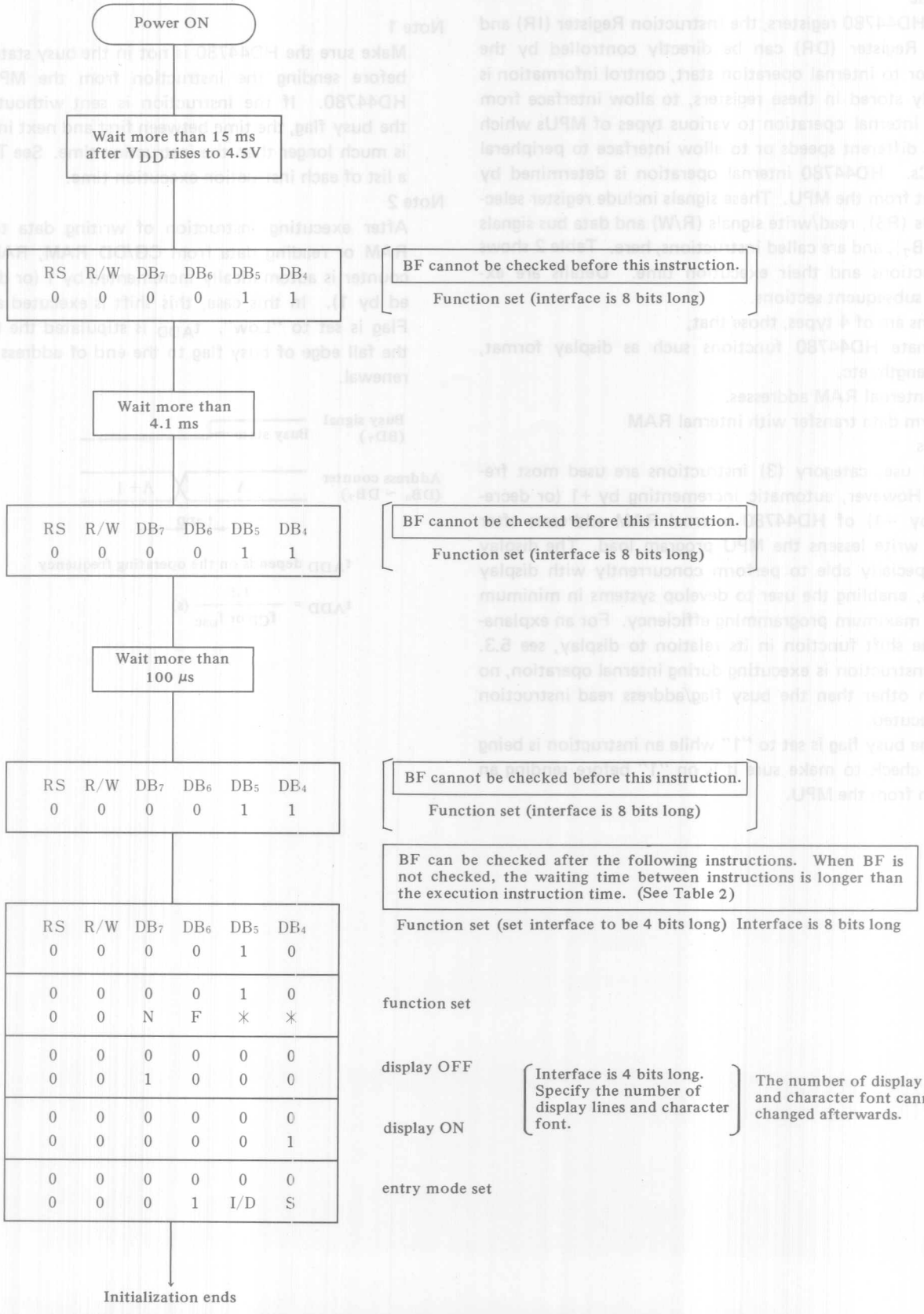
If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required.

Use the following procedure for initialization.

(1) When interface is 8 bits long;



(2) When interface is 4 bits long



5. Instruction

5.1 Outline

Only two HD44780 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD44780 internal operation to various types of MPUs which operate in different speeds or to allow interface to peripheral control ICs. HD44780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals ($DB_0 \sim DB_7$), and are called instructions, here. Table 2 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

(1) Designate HD44780 functions such as display format, data length, etc.
(2) Give internal RAM addresses.
(3) Perform data transfer with internal RAM
(4) Others

In normal use, category (3) instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by −1) of HD44780 internal RAM addresses after each data write lessens the MPU program load. The display shift is especially able to perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programming efficiency. For an explanation of the shift function in its relation to display, see 5.3.

When an instruction is executing during internal operation, no instruction other than the busy flag/address read instruction will be executed.

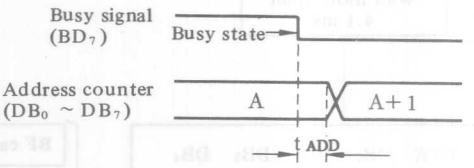
Because the busy flag is set to "1" while an instruction is being executed, check to make sure it is on "1" before sending an instruction from the MPU.

Note 1

Make sure the HD44780 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD44780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See Table 2 for a list of each instruction execution time.

Note 2

After executing instruction of writing data to CG/DD RAM or reading data from CG/DD RAM, RAM address counter is automatically incremented by 1 (or decremented by 1). In this case, this shift is executed after Busy Flag is set to "Low". t_{ADD} is stipulated the time from the fall edge of busy flag to the end of address counter's renewal.



t_{ADD} depends on the operating frequency

$$t_{ADD} = \frac{1.5}{f_{CP} \text{ or } f_{osc}} \text{ (s)}$$

Table 2 Instructions

Instruction	Code										Description	Execution time (when fosc is 250 kHz) Note 1	Execution time (when fosc is 160 kHz) Note 2
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	82 μs ~ 1.64 ms	120 μs ~ 4.9 ms
Return home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	40 μs ~ 1.6 ms	120 μs ~ 4.8 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40 μs	120 μs
Display ON/ OFF control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 μs	120 μs
Cursor and display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents	40 μs	120 μs
Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL) number of display lines (L) and character font (F).	40 μs	120 μs
Set CG RAM address.	0	0	0	1	A_{CG}						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs	120 μs
Set DD RAM address	0	0	1	A_{DD}							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs	120 μs
Read busy flag & address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	1μs	1 μs
Write data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs	120 μs
Read data to CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs	120 μs
	I/D = 1: Increment (+1) I/D = 0: Decrement (−1) S = 1: Accompanies display shift. S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right. R/L = 0: Shift to the left. DL = 1: 8 bits DL = 0: 4 bits N = 1: 2 lines N = 0: 1 line F = 1: 5 x 10 dots F = 0: 5 x 7 dots BF = 1: Internally operating BF = 0: Can accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address Corresponds to cursor address. AC: Address counter used for both of DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fosc is 270 kHz: $40\ \mu s \times \frac{250}{270} = 37\ \mu s$	

* No effect

5.2 Description of details

(1) Clear display

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	1

Writes space code "20" (hexadecimal) (character pattern for character code "20" must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the display (the first line if 2 lines are displayed). Set I/D = 1 (Increment Mode) of Entry Mode. S of Entry Mode doesn't change.

(2) Return home

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	*

* No effect

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

(3) Entry mode set

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM does it shift when S = 0.

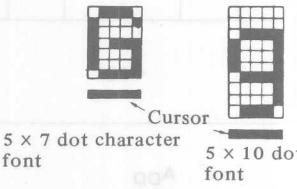
(4) Display ON/OFF control

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

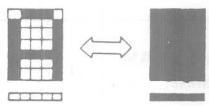
D: The display is ON when D = 1 and OFF when D = 0. When off due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor displays when C = 1 and does not display when C = 0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 x 7 dot character font is selected and 5 dots in the 11th line when the 5 x 10 dot character font is selected.

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all blank dots and display characters at 409.6 ms interval when f_{CP} or f_{osc} = 250 kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of f_{CP} or f_{osc}. $409.6 \times \frac{250}{270} = 379.2$ ms when f_{CP} = 270 kHz.)



(a) Cursor Display Example



(b) Blink Display Example

(5) Cursor or display shift

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* No effect

Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line position.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Address counter (AC) contents do not change if the only action performed is shift display.

(6) Function set

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	1	DL	N	F	*	*

* No effect

DL: Sets interface data length. Data is sent or received in 8 bit lengths ($DB_7 \sim DB_0$) when DL = 1 and in 4 bit lengths ($DB_7 \sim DB_4$) when DL = 0.
When the 4 bit length is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

(Note) Perform the function at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

N	F	No. of display lines	Character font	Duty factor	Remarks
0	0	1	5 x 7 dots	1/8	
0	1	1	5 x 10 dots	1/11	
1	*	2	5 x 7 dots	1/16	Cannot display 2 lines with 5 x 10 dot character font.

* No effect

(7) Set CG RAM address

	RS	R/W	DB_7						DB_0
Code	0	0	0	1	A	A	A	A	A	A

← Higher Order Bits Lower Order Bits →

Sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

(8) Set DD RAM address

	RS	R/W	DB_7						DB_0
Code	0	0	1	A	A	A	A	A	A	A

← Higher Order Bits lower Order Bits →

Sets the DD RAM address into the address counter in binary AAAAAAA. Data is then written or read from the MPU for the DD RAM.
However, when N = 0 (1-line display), AAAAAAA is "00" ~ "4F" (hexadecimal),
when N = 1 (2-line display), AAAAAAA is "00" ~ "27" (hexadecimal) for the first line, and "40" ~ "67" (hexadecimal) for the second line.

(9) Read busy flag & address

	RS	R/W	DB_7						DB_0
Code	0	1	BF	A	A	A	A	A	A	A

← Higher Order Bits Lower Order Bits →

Reads the busy flag (BF) that indicates the system is now internally operating by a previously received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to "0". Check the BF status before the next wire operation.
At the same time, the value of the address counter expressed in binary AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in Items (7) and (8).

(10) Write data to CG or DD RAM

	RS	R/W	DB_7						DB_0
Code	1	0	D	D	D	D	D	D	D	D

← Higher Order Bits Lower Order Bits →

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM. Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

(11) Read data from CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D
			← Higher Order Bits					Lower Order Bits →		

Reads binary 8 bit data DDDDDDDD from the CG or DD RAM. The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing the "read" instruction, the next address data is normally read from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

(Note) The address counter (AC) is automatically incremented or decremented by 1 after "write" instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot than be read out even if "read" instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), just before reading out execute the "read" instruction from the second time the "read" instruction is serial.

5.3 Instruction and display correspondence

(1) 8-bit operation, 8-digit x 1-line display (using internal reset)

Following table shows an example of 8-bit x 1-line display in 8-bit operation.

The HD44780 functions must be set by Function Set prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like the lightening board when combined with display shift operation.

Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

8 bit operation, 8-digit 1-line display example (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display lines and character font. (Number of display lines and character fonts cannot be changed hereafter.)
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI_	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	·HITACHI_	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI_	Writes "Space".
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M_	Writes "M".
12	⋮	⋮	
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO_	Writes "0".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Diaplay Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO_	Shifts display and cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM_	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (Address 0).

(2) 4-bit operation, 8-digit x 1-line display (using internal reset)

The program must set functions prior to 4-bit operation. The following table shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to $DB_0 \sim DB_3$, a rewrite is then required. However, since one operation is completed in two access of 4-bit operation, a rewrite is needed as a function (see the following table).

Thus, $DB_4 \sim DB_7$ of the function set is written twice.

4 bit operation, 8-digit 1-line display (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets 4-bit operation and selects 1-line display and 5 x 7 dot character font. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character fonts cannot be changed hereafter.)
4	Display ON/OFF Control 0 0 0 0 0 0 0 0 1 1 1 0	—	Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0	—	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H—	Writes "H". The cursor is incremented by one and shifts to the right.

Hereafter, control is the same as 8-bit operation.

(3) 8-bit operation, 8-digit x 2-line display

For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must again be set after the 8th character is completed. (See the following table) Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second display will only move within each line many times.

8 bit operation, 8-digit x 2-line display example (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 — DB_0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and 5 x 7 dot character font.
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift are operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

6. Precaution on programming

(1) Instruction of function set

Perform the function at the head of program that accesses HD44780 before executing all instructions, and not change the data of the Instruction Register in the program. The data of function register can be changed by the program as follows;

a. • Changing of DL (Data Length)
   • Perform the instruction appointed in 4.2 (2), when DL is changed from 8-bit length to 4-bit length mode.
   • Perform the instruction appointed in 4.2 (1), when DL is changed from 4-bit length to 8-bit length mode.

b. • Changing of N (Column Number)
   • Perform the instruction of function set after executing instruction of display clear or display off.

In this case, sequence of AC and DD RAM must be changed. Thus, rewrite the address set register after that.

c. • Changing of F (Font)
   • There is no problem in this case, but for dual-line display, the font mode of 5 x 11 cannot be selected (this mode is forbidden by hardware).

When N or F is changed, power supply voltage for LCD must be changed. If not changed, crosstalk will appear, or contrast will be poor.

(2) Busy flag check

HD44780 is produced in the CMOS process, therefore internal executing time is long. Standard time is 40 μs ~ 1.6 ms. (This varies by instruction)

When the high speed MPU controls it, check the busy flag before performing instruction or reading data.

While internal operation is active, Enable signal is not accepted. (Enable signal at reading status register for checking busy flag is accepted) Busy flag signal is output through DB_7, as shown in Table 3, when RS = "0", R/W = "1", and Enable = "1".

(3) Input of unidentified instruction code

Undefined instruction code of HD44780 is only as follows;

RS	R/W	DB_7 ~ DB
0	0	0 ~

(Others are included to defined instruction)

When the undefined instruction code is loaded to HD44780, it accepts the code, but does not change the internal states (RAM and other status of Flags). Busy state, however continues for maximum 40 μs by the acceptance of the code.

Table 3 The relation between the operation and the combination of RS, R/W

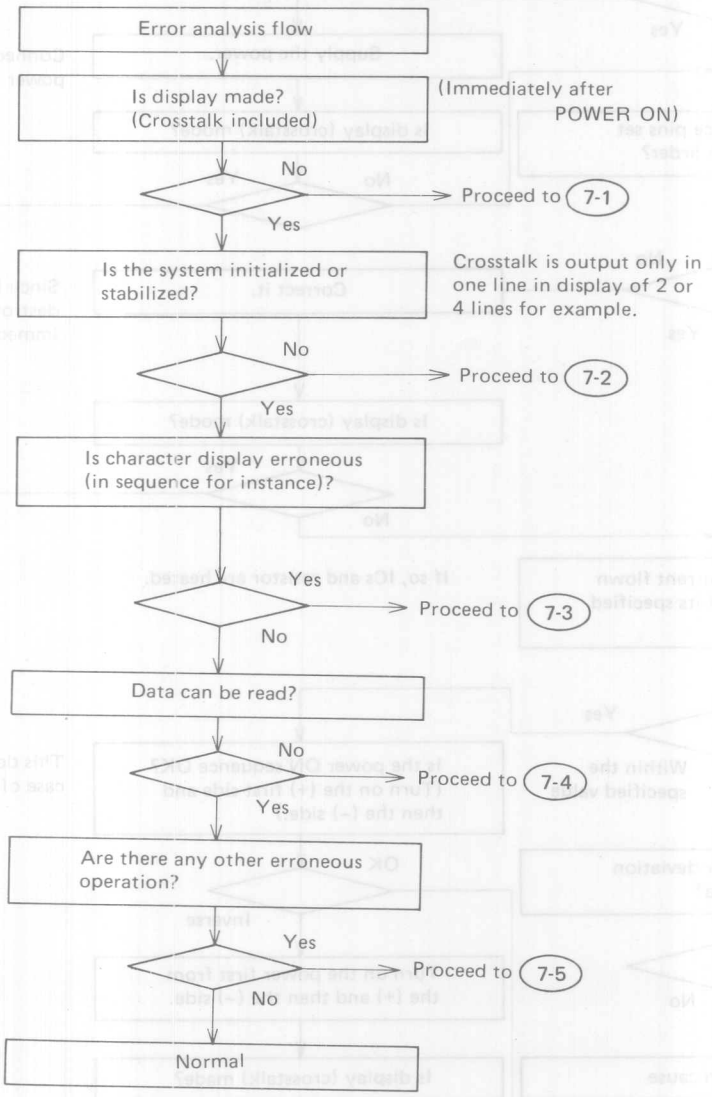
RS	RW	E	OPERATION
0	0		Write instruction code
0	1		Read busy flag and address counter
1	0		Write data
1	1		Read data

When performing data and instruction code by 4 bit, transfer RS, R/W every time.

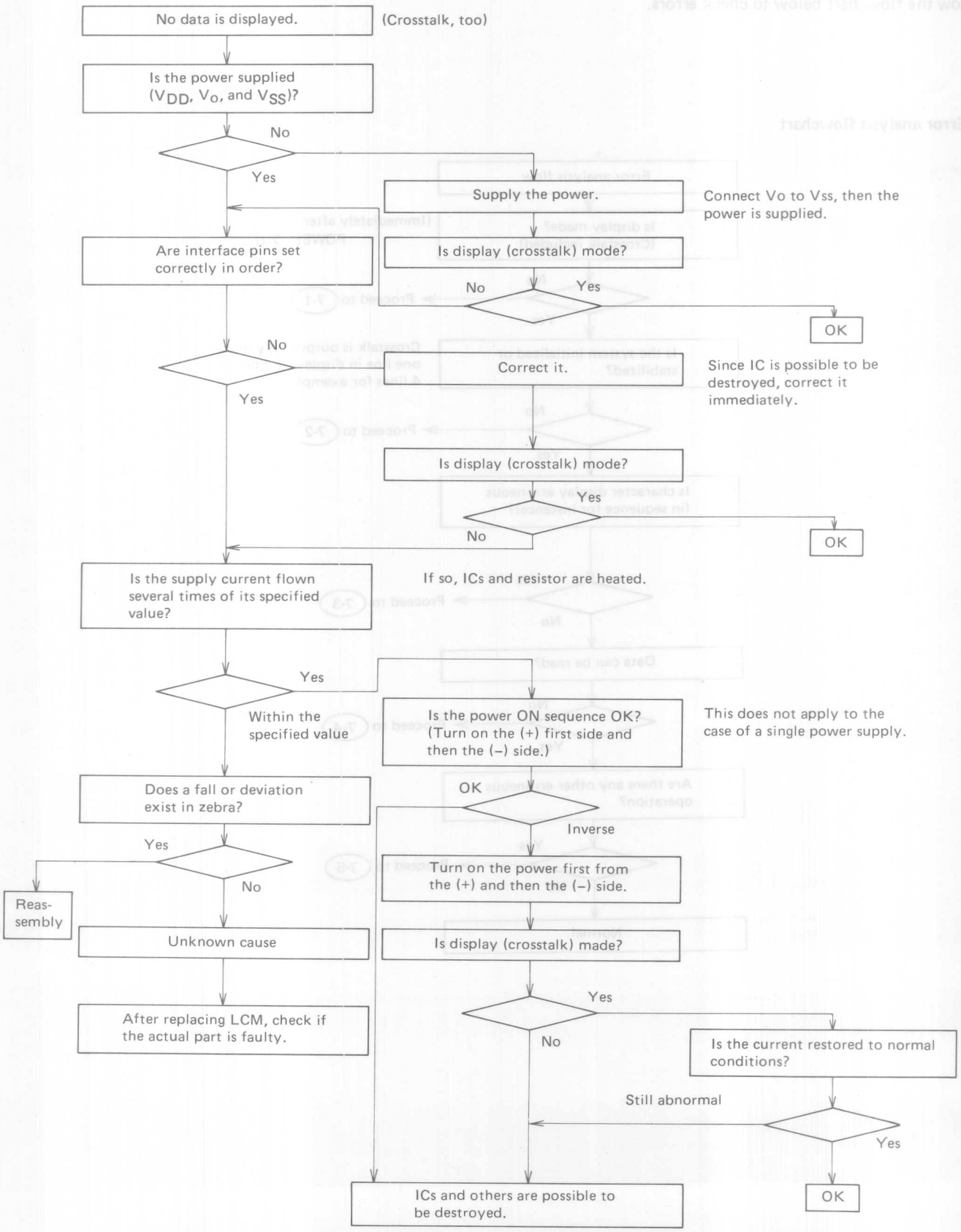
7. How to check trouble

Follow the flowchart below to check errors.

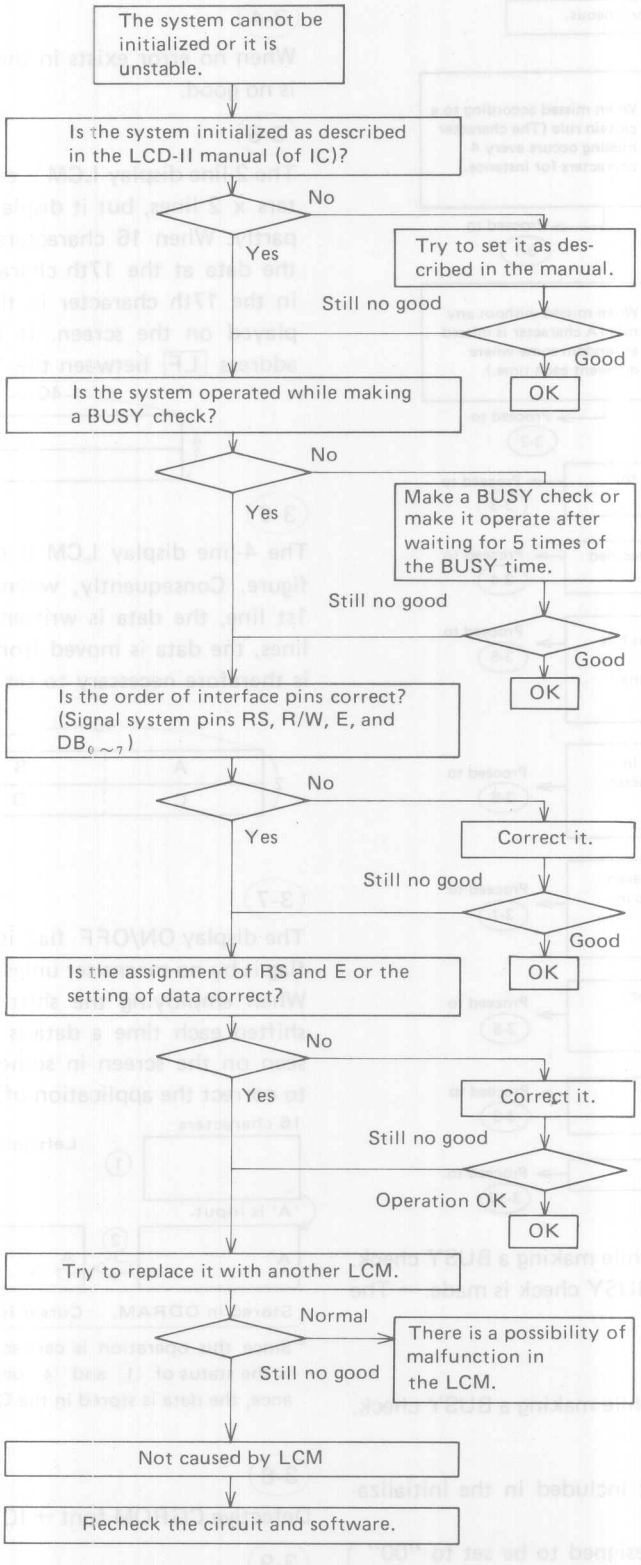
■ **Error analysis flowchart**



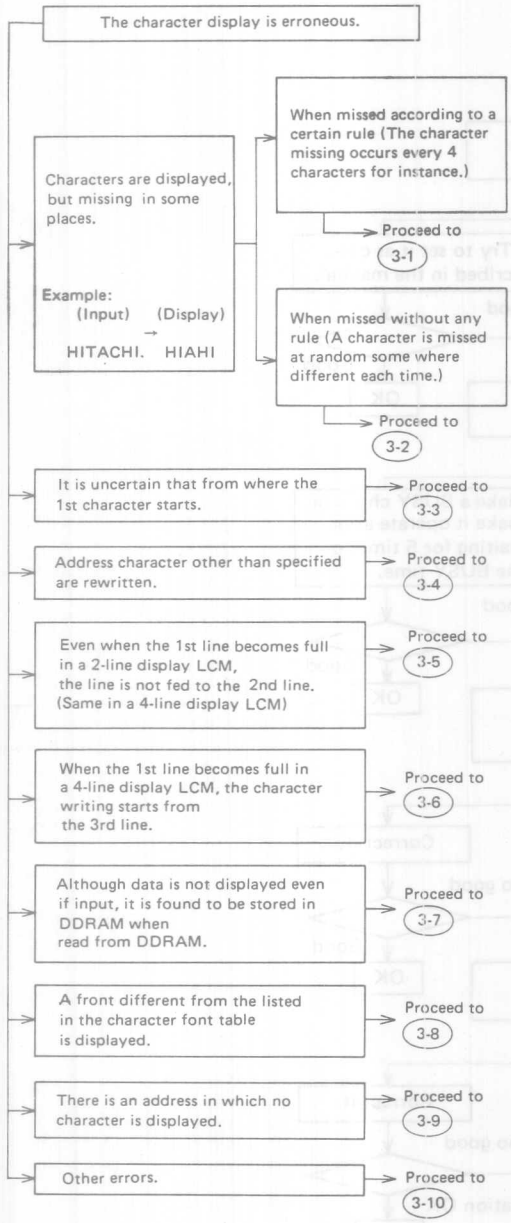
7.1 No data is displayed (Crosstalk too)



7.2 The system cannot be initialized or it is unstable.



7.3 The character display is erroneous.



(3-1)

Data is fed too fast. → Retry it while making a BUSY check. It is still too fast even when the BUSY check is made. → The function of LCD-II is no good.

(3-2)

Data is fed too fast. → Retry it while making a BUSY check.

(3-3)

The address Set command is not included in the initialization.

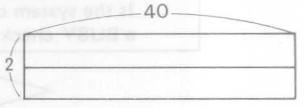
→ Although the address is so designed to be set to "00" at the power ON according to the Power ON Reset function of the LCD-II itself, this Power ON Reset function does not work in some cases according to the power ON conditions.

(3-4)

When no error exists in the software, the function of LCD-II is no good.

(3-5)

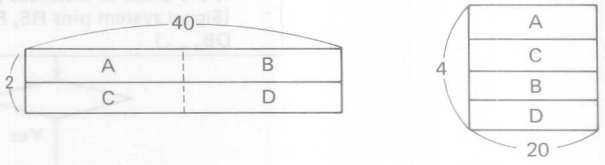
The 2-line display LCM is electrically composed of 40 characters x 2 lines, but it displays 16 characters or 20 characters partly. When 16 characters are written (in the 1st line) and the data at the 17th character is input as it is, it is entered in the 17th character in the 1st line and its is neither displayed on the screen. It is therefore necessary to set the address [LF] between the 16th caracter and 17th character.



[LF] : line feed

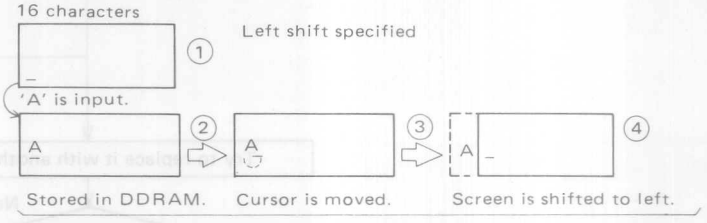
(3-6)

The 4-line display LCM is composed as shown in the right figure. Consequently, when written continuously from the 1st line, the data is written as A → B. When displayed in 4 lines, the data is moved from the 1st line to the 3rd line. It is therefore necessary to set the address of [LF] in this case.



(3-7)

The display ON/OFF flag is turned to the OFF side. (This flag is by no means set unless turned to the ON side.)
When employing the shift function together, the screen is shifted each time a data is written and the data can not be seen on the screen in some cases. It is therefore necessary to correct the application of the shift function.



* Since this operation is carried out in a moment, what can be seen is the status of ① and ④ only. Although not displayed in appearance, the data is stored in the DDRAM.

(3-8)

Defective CGROM font → IC is faulty.

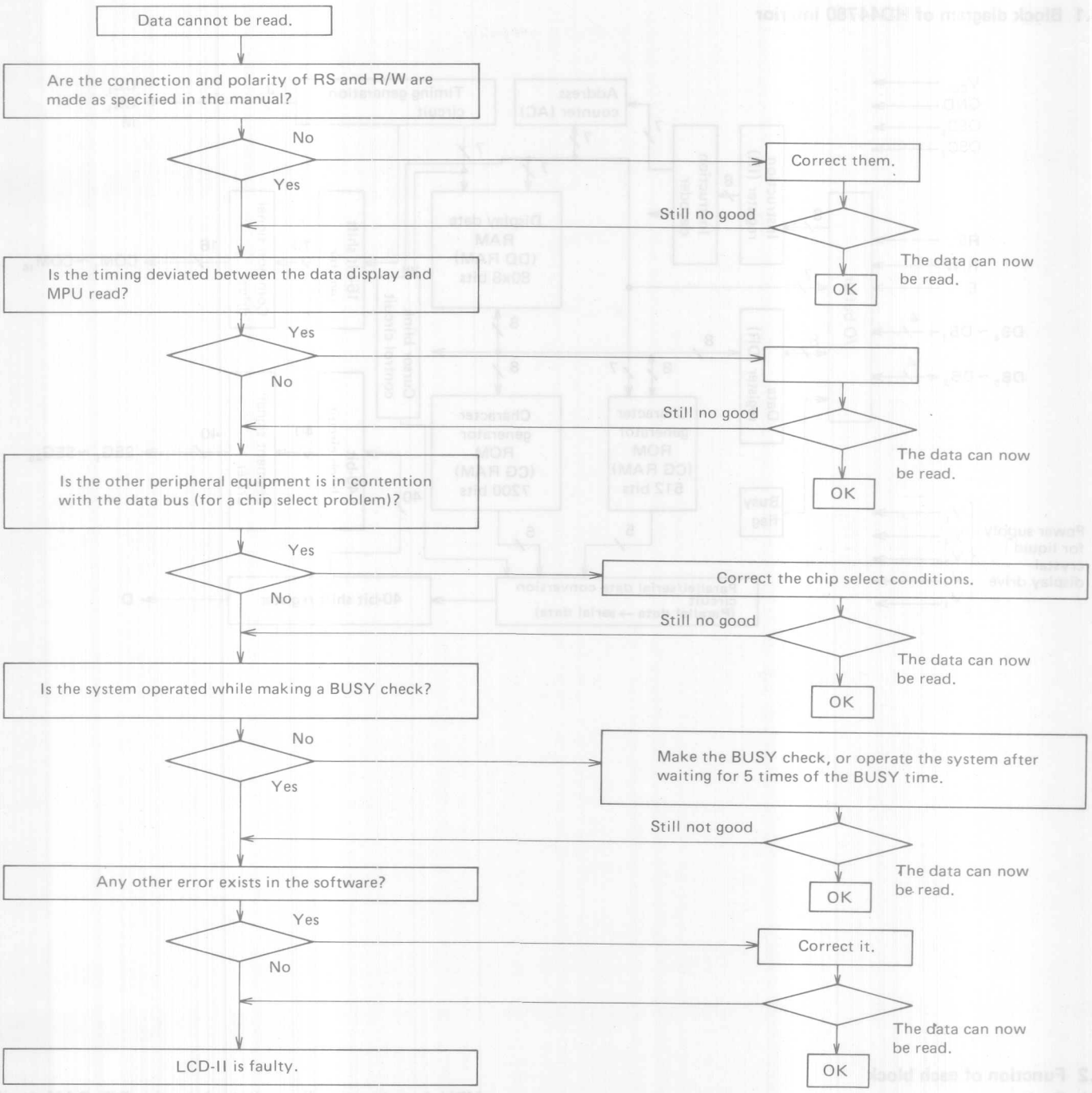
(3-9)

If no error exists in the software, the IC is faulty.

(3-10)

Contact our agent for any other erroneous event.

7.4 Data cannot be read



7.5 Others

Others

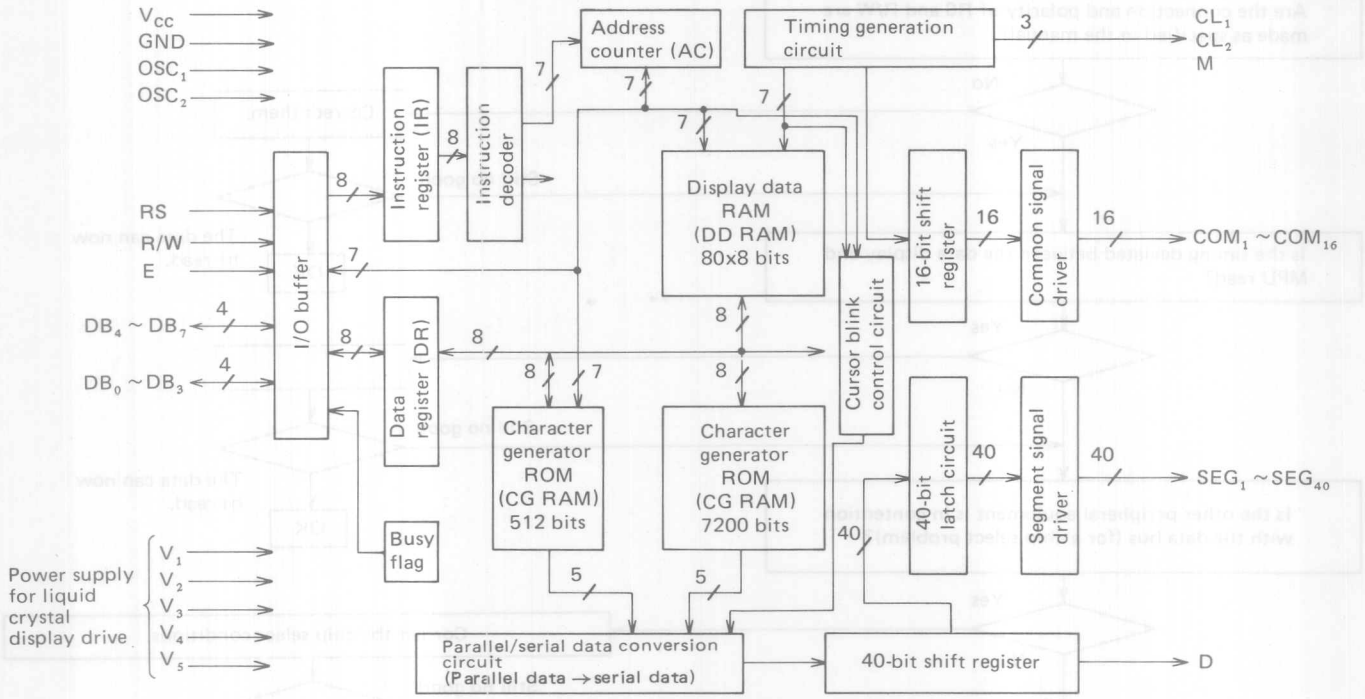
↓

Check the following:

- Use conditions
- Erroneous events
- Contents of operation before and after the error event occurrence
- Flowchart, if possible. (The program, if given, can not be decoded.)

8. Block diagram and function of each block

8.1 Block diagram of HD44780 interior



8.2 Function of each block

(1) Register

The HD44780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Table 4 Register selection

RS	R/W	E	Operation
0	0	⌐	IR write as internal operation (Display clear, etc.)
0	1	⌐‾¬	Read busy flag (DB_7) and address counter ($DB_0 \sim DB_6$)
1	0	⌐	DR write as internal operation (DR to DD or CG RAM)
1	1	⌐‾¬	DR read as internal operation (DD or CG RAM to DR)

(2) Busy flag (BF)

When the busy flag is "1", the HD44780 is in the internal operation mode, and the next instruction will not be accepted. As Table 4 shows, the busy flag is output to DB_7 when RS = 0 and R/W = 1. The next instruction must be written after ensuring that the busy flag is "0".

(3) Address counter (AC)

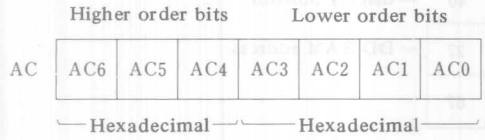
The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by −1). AC contents are output $DB_0 \sim DB_6$ when RS = 0 and R/W = 1, as shown in Table 4.

(4) Display data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 x 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

The DD RAM address (A_{DD}) is set in the Address Counter (AC) and is represented in hexadecimal.



(Ex.) DD RAM address "4E"

1	0	0	1	1	1	0
← 4 →			← E →			

1-line display (N = 0)

	1	2	3	4	5					79	80	← display position
1-line	00	01	02	03	04					4E	4F	← DD RAM address

(a) When the display characters are less than 80, the display begins at the head position. For example, 8 characters using one HD44780 are displayed as:

	1	2	3	4	5	6	7	8	← display position
1-line	00	01	02	03	04	05	06	07	← DD RAM address

When the display shift operation is performed, the DD RAM address moves as:

01	02	03	04	05	06	07	08	(Left shift display)
4F	00	01	02	03	04	05	06	(Right shift display)

(b) 16-character display using an HD44780 and an HD44100H is as shown below:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM address

HD44780 display — HD44100H display

When the display shift operation is performed, the DD RAM address moves as:

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	(Left shift display)
4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	(Right shift display)

(c) The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD44780 and two or more HD44100H's can be considered an extension of (b). Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100H's.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	73	74	75	76	77	78	79	80	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	48	49	4A	4B	4C	4D	4E	4F	← DD RAM address

HD44780 display — HD44100H (1) display — HD44100H (2) ~ (8) display — HD44100H (9) display

2-line display (N = 1)

	1	2	3	4	5	.....	39	40	← display position
1-line	00	01	02	03	04	.....	26	27	← DD RAM address
2-line	40	41	42	43	44	.....	66	67	

(a) When the number of display characters is less than 40 x 2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44780 is used, 8 characters x 2 lines are displayed as:

	1	2	3	4	5	6	7	8	← display position
1-line	00	01	02	03	04	05	06	07	← DD RAM address
2-line	40	41	42	43	44	45	46	47	

When display shift is performed, the DD RAM address move as:

01	02	03	04	05	06	07	08	(Left shift display)
41	42	43	44	45	46	47	48	

27	00	01	02	03	04	05	06	(Right shift display)
67	40	41	42	43	44	45	46	

(b) 16 character x 2 line are displayed when an HD44780 and an HD44100H are used.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

HD44780 display — HD44100H display

When display shift is performed, the DD RAM address moves as follows:

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Left shift display)

27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

(Right shift display)

(c) The relation between display position and DD RAM address when the number of display digits is increased by using one HD44780 and two or more HD44100H's, can be considered an extension of (b).

Since the increase can be 8 digits x 2 lines for each additional HD44100H, up to 40 digits x 2 lines can be displayed by connecting 4 HD44780's externally.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	.....	33	34	35	36	37	38	39	40	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	.....	20	21	22	23	24	25	26	27	← DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	.....	60	61	62	63	64	65	66	67	

└HD44780 display┘ └HD44100 (1) display┘ └HD44100H (2) (3) display┘ └HD44100H (4)┘

(d) Display position and DD RAM address for LM020L.

Character NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM address	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47

(Note) Shift display is as same as that of 8 char. x 2 line type.

(e) Display position and DD RAM address for LM041L.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	
3-line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
4-line	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	

(f) Display position and DD RAM address for LM044L.

	1桁	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	←display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	←DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	
3-line	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	
4-line	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67	

(Note) Shift display is as same as 2-line type.

(5) Character generator ROM (CG ROM)

The character generator ROM generates 5 x 7 dot or 5 x 10 dot character patterns from 8-bit character codes. It can generate 160 types of 5 x 7 dot character patterns and 32 types of 5 x 10 dot character patterns. Tables 5 (1) and 5 (2) show the relation between character codes and character patterns in the Hitachi standard HD44780A00. User defined character patterns are also available by mask-programming ROM. For details, see "The LCD-II (HD44780) Breadboard User's Manual".

(6) Character generator RAM (CG RAM)

The character generator RAM is the RAM with which the user can rewrite character patterns by program. With 5 x 7 dots, 8 types of character patterns can be written and with 5 x 10 dots 4 types can be written. Write the character codes in the left columns of Tables 6 (1) and 6 (2) to display character patterns stored in CG RAM.

Table 5 shows the relation between CG RAM addresses and data and display patterns.

As Table 5 shows, an area that is not used for display can be used as a general data RAM.

(7) Timing generation circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

(8) Liquid crystal display driver circuit

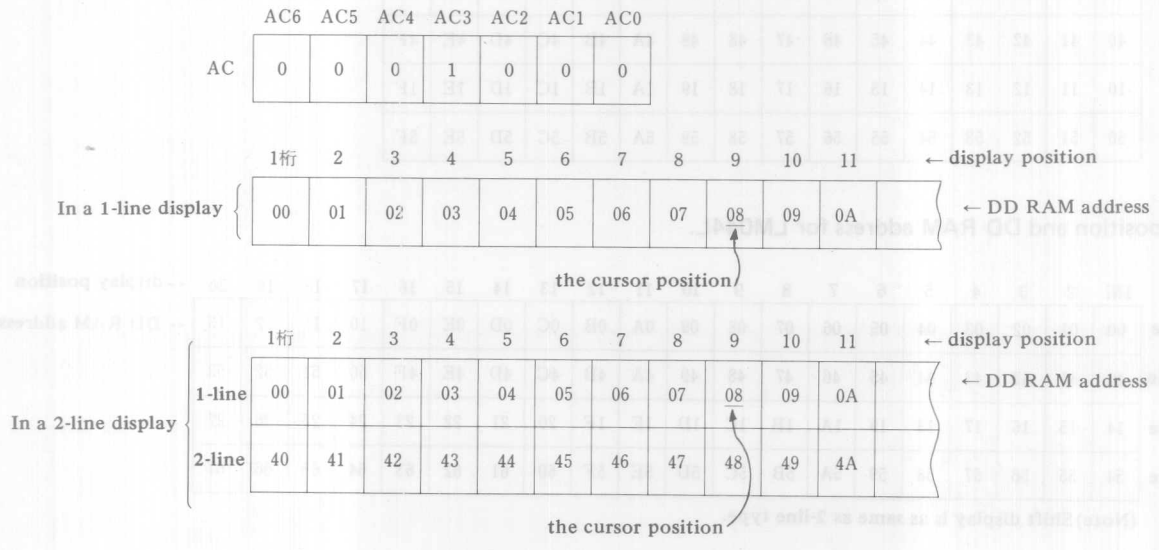
The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms. The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data is sent to the HD44100H, externally connected in cascade, used for display digit number extension. Send of serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM). Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD44780 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

(9) Cursor/Blink control circuit

This is the circuit that generates the cursor or blink. The cursor or the blink appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).

When the address counter is $(08)_{16}$, a cursor position is:

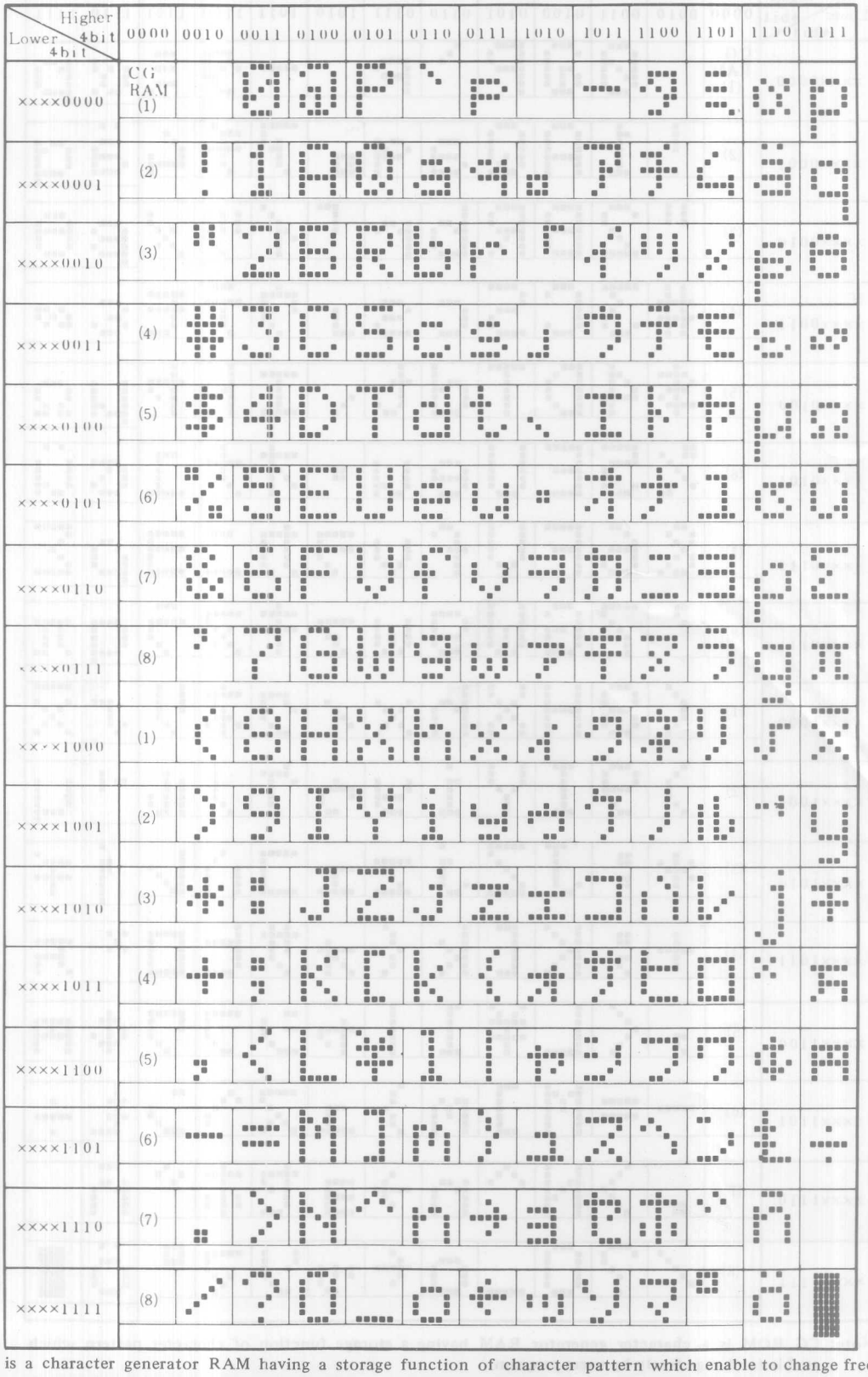


(Note) The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

Table 5

CORRESPONDENCE BETWEEN CHARACTER CODES AND CHARACTER PATTERN

(1) 5 x 10 dot, applied type: H2570, H2571, H2572, LM027



Note 1. CG RAM is a character generator RAM having a storage function of character pattern which enable to change freely by users program.
Note 2. When line setting at initialization is 2 lines (N = 1), pattern becomes 5 x 7 dot.

(2) 5 x 7 dot, applied type: LM054, H2570, LM015, LM568AF, LM020L, LM070L, LM038, LM027, H2571, H2572, LM058, LM052L, LM016L, LM032L, LM060L, LM017L, LM018L, LM041L, LM044L

Note: CG ROM is a character generator RAM having a storage function of character pattern which enable to change freely by users program.

Table 6 Relation between CG RAM addresses and character code (DD RAM) and character pattern (CG RAM data).

(1) For 5 x 7 dot character pattern

Character Codes (DD RAM Data) 7 6 5 4 3 2 1 0 ←Higher Lower→	CG RAM Address 5 4 3 2 1 0 ←Higher Lower→	Character Patterns (CG RAM Data) 7 6 5 4 3 2 1 0 ←Higher Lower→	
0 0 0 0 ✳ 0 0 0	0 0 0	✳ ✳ ✳ 1 1 1 1 0	Character Pattern Example (1)
	0 0 1	1 0 0 0 1	
	0 1 0	1 0 0 0 1	
	0 1 1	1 1 1 1 0	
	1 0 0	1 0 1 0 0	
	1 0 1	1 0 0 1 0	
	1 1 0	1 0 0 0 1	
	1 1 1	✳ ✳ ✳ 0 0 0 0 0	← Cursor Position
0 0 0 0 ✳ 0 0 1	0 0 0	✳ ✳ ✳ 1 0 0 0 1	
	0 0 1	0 1 0 1 0	Character Pattern Example (2)
	0 1 0	1 1 1 1 1	
	0 1 1	0 0 1 0 0	
	1 0 0	1 1 1 1 1	
	1 0 1	0 0 1 0 0	
	1 1 0	0 0 1 0 0	
	1 1 1	✳ ✳ ✳ 0 0 0 0 0	
0 0 0 0 ✳ 1 1 1	0 0 0	✳ ✳ ✳	✳ No effect
	0 0 1		
	1 0 0		
	1 0 1		
	1 1 0		
	1 1 1	✳ ✳ ✳	

(Note) 1: Character code bits 0 ~ 2 correspond to CG RAM address bits 3 ~ 5 (3 bits: 8 types).

2: CG RAM address bits 0 ~ 2 designate character pattern line position. The 8th line is the cursor position and display is performed in logical OR by the cursor.
Maintain the 8th line data, corresponding to the cursor display position, in the "0" state for cursor display. When the 8th line data is "1", bit 1 lights up regardless of cursor existence.

3: Character pattern row positions correspond to CG RAM data bits 0 ~ 4, as shown in the figure (bit 4 being at the left end). Since CG RAM data bits 5 ~ 7 are not used for display, they can be used for the general data RAM.

4: As shown in Tables 3 and 4, CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 3 is a ineffective bit, the "R" display in the character pattern example, is selected by character code "00" (hexadecimal) or "08" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(2) For 5 x 10 dot character pattern

Character Codes (DD RAM Data) 7 6 5 4 3 2 1 0 ←Higher Lower→	CG RAM Address 5 4 3 2 1 0 ←Higher Lower→	Character Patterns (CG RAM Data) 7 6 5 4 3 2 1 0 ←Higher Lower→	
0 0 0 0 ✳ 0 0 ✳	0 0 0 0 0 0	✳ ✳ ✳ 0 0 0 0 0	Character Pattern Example
	0 0 0 1	0 0 0 0 0	
	0 0 1 0	1 0 1 1 0	
	0 0 1 1	1 1 0 0 1	
	0 1 0 0	1 0 0 0 1	
	0 1 0 1	1 0 0 0 1	
	0 1 1 0	1 1 1 1 0	
	0 1 1 1	1 0 0 0 0	
	1 0 0 0	1 0 0 0 0	
	1 0 0 1	1 0 0 0 0	
	1 0 1 0	✳ ✳ ✳ 0 0 0 0 0	← Cursor Position
	1 0 1 1	✳ ✳ ✳ ✳ ✳ ✳ ✳ ✳	
	1 1 0 0		
	1 1 0 1		
	1 1 1 0		
	1 1 1 1	✳ ✳ ✳ ✳ ✳ ✳ ✳ ✳	
	0 0 0 0	✳ ✳ ✳	
	0 0 0 1		
0 0 0 0 ✳ 1 1 ✳	1 1 1 0 0 1		
	1 0 1 0	✳ ✳ ✳	
	1 0 1 1	✳ ✳ ✳ ✳ ✳ ✳ ✳ ✳	
	1 1 0 0		
	1 1 0 1		✳ No effect
	1 1 1 0		
	1 1 1 1	✳ ✳ ✳ ✳ ✳ ✳ ✳ ✳	

(Note) 1: Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).

2: CG RAM address bits 0 ~ 3 designate character pattern line position. The 11th line is the cursor position and display is performed in logical OR with cursor.
Maintain the 11th line data corresponding to the cursor display position in the "0" state for cursor display. When the 11th line data is "1", bit 1 lights up regardless of cursor existence. Since the 12th ~ 16th lines are not used for display, they can be used for the general data RAM.

3: Character pattern row positions are the same as 5 x 7 dot character pattern positions.

4: CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 0 and 3 are ineffective bits, "P" display in the character pattern example is selected by character code "00", "01", "08" and "09" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.